PHYSIQUE DES COMPOSANTS SEMI-CONDUCTEURS

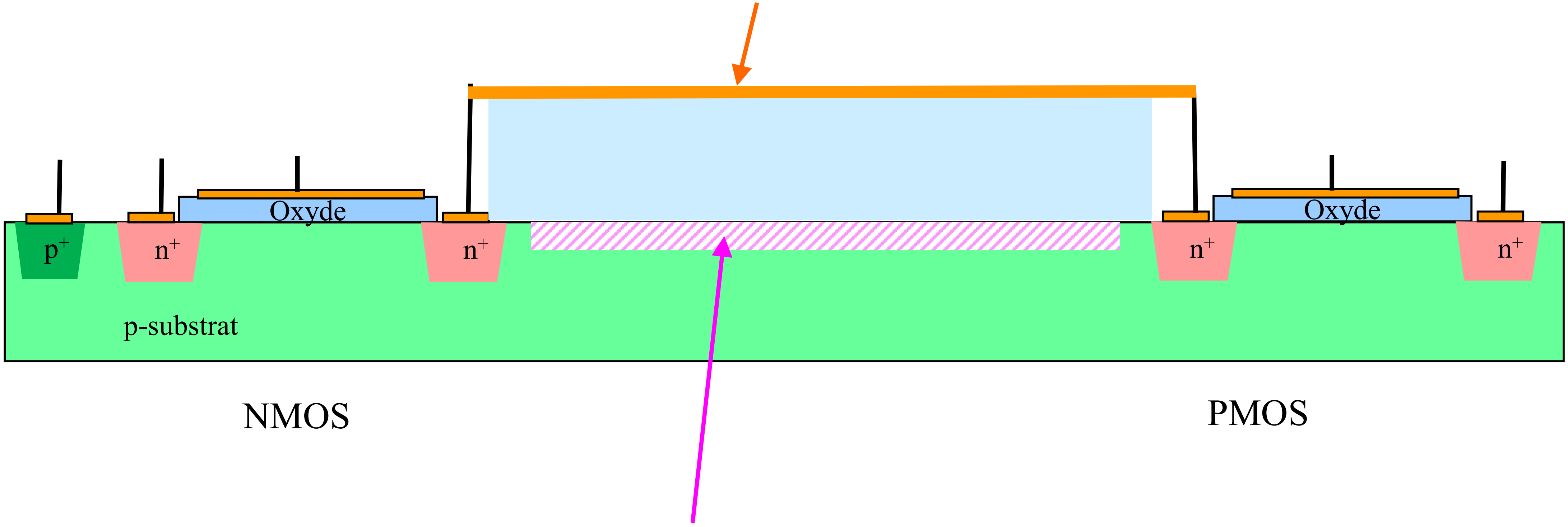
XI) FET: partie 2
technologie et mémoires non-volatiles

P.A. Besse

EPFL

Structure MOSFET

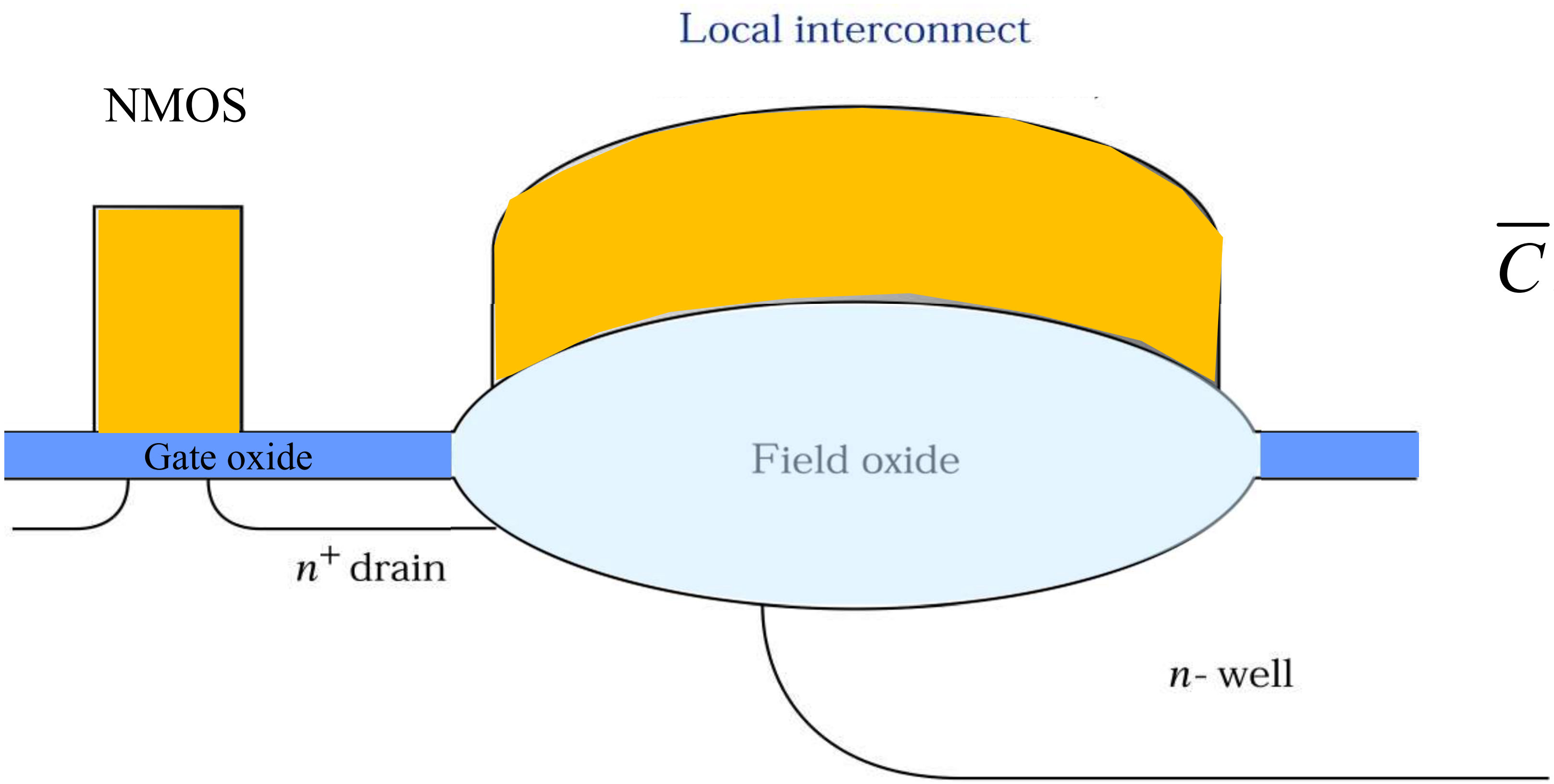
Relier en évitant la formation d'un canal !!



⇒ **Augmenter fortement le threshold VT**

11.1 contrôle de la tension de threshold: Oxyde de champ

Semiconductor Devices, 2/E by S. M. Sze



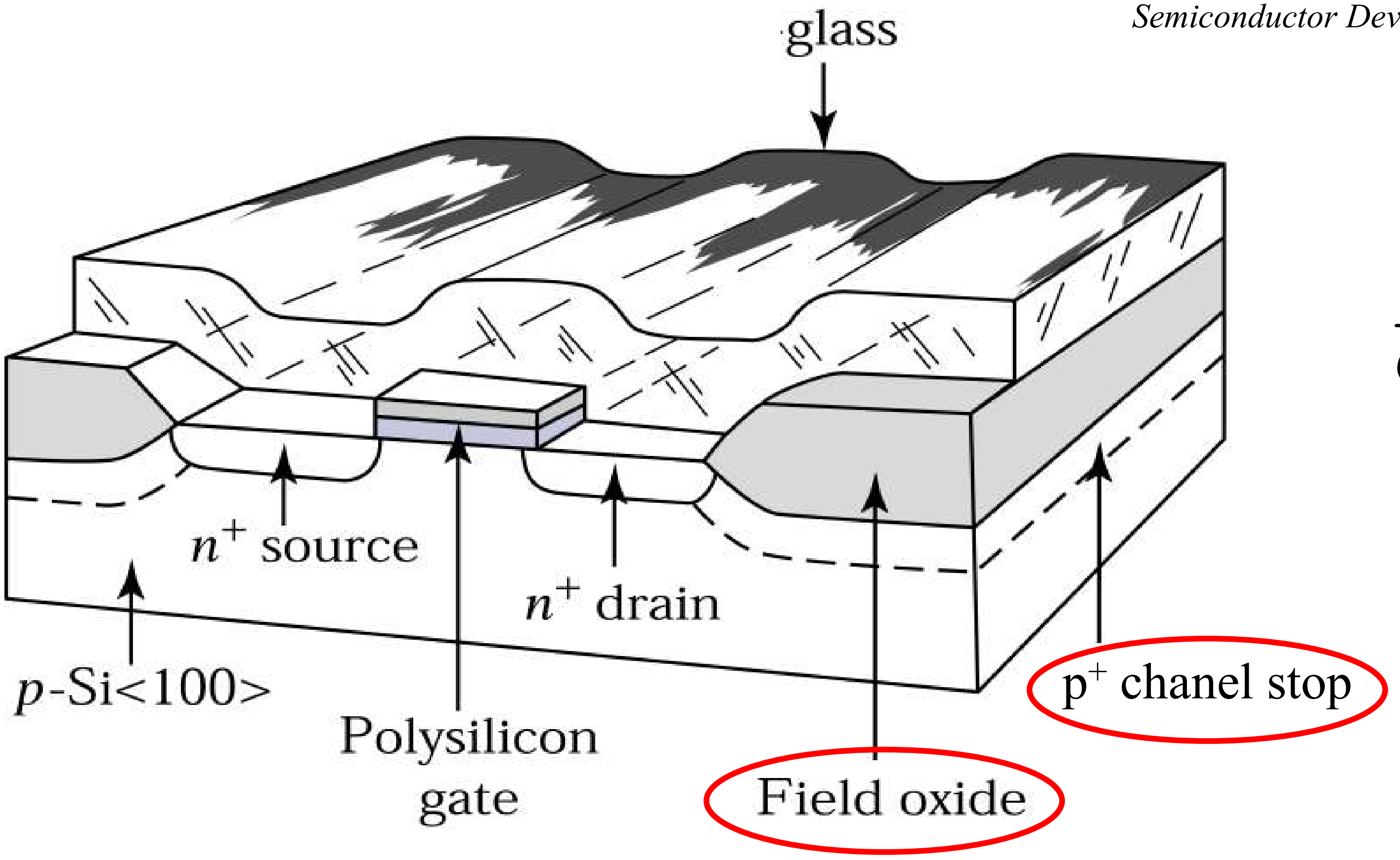
$$\overline{C}_{ox} = \frac{\varepsilon_0 \varepsilon_{ox}}{d_{ox}}$$

$$V_{M0} = V_{fb} + 2\psi_B \left(1 + 2\frac{C_{B,th}}{C_{ox}} \right)$$

Maximaliser V_{M0} par un oxyde épais
→ Éviter un canal « parasite ».

Chanel stop

Semiconductor Devices, 2/E by S. M. Sze

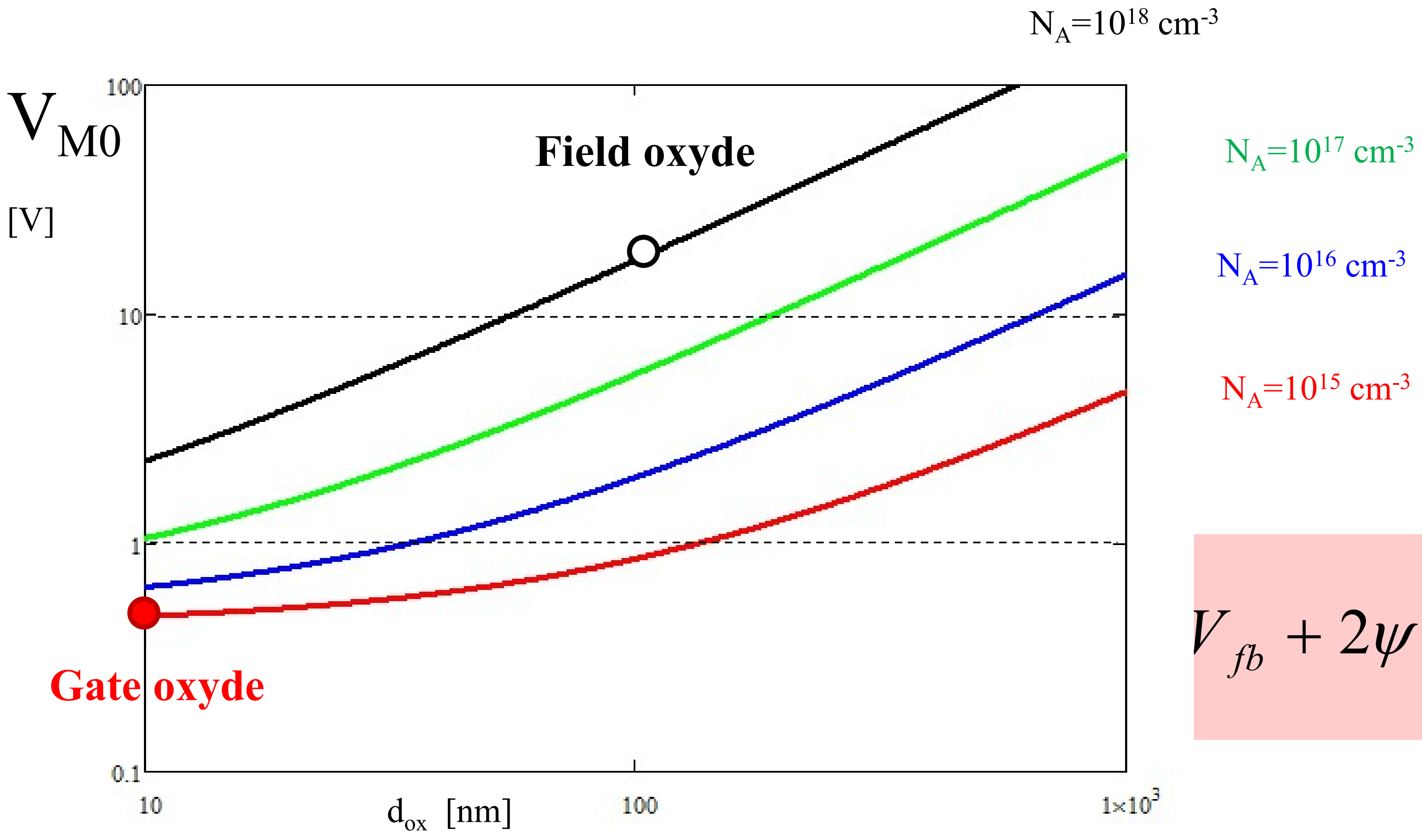


$$\overline{C}_{B,th} = \frac{1}{2}\frac{\sqrt{2\varepsilon_0\varepsilon_s q N_A}}{\sqrt{2\psi_B}}$$

$$V_{M0} = V_{fb} + 2\psi_B\left(1 + 2\frac{C_{B,th}}{C_{ox}}\right)$$

Maximaliser V_{M0} par une zone fortement dopée p (N_A grand) = « chanel stop »

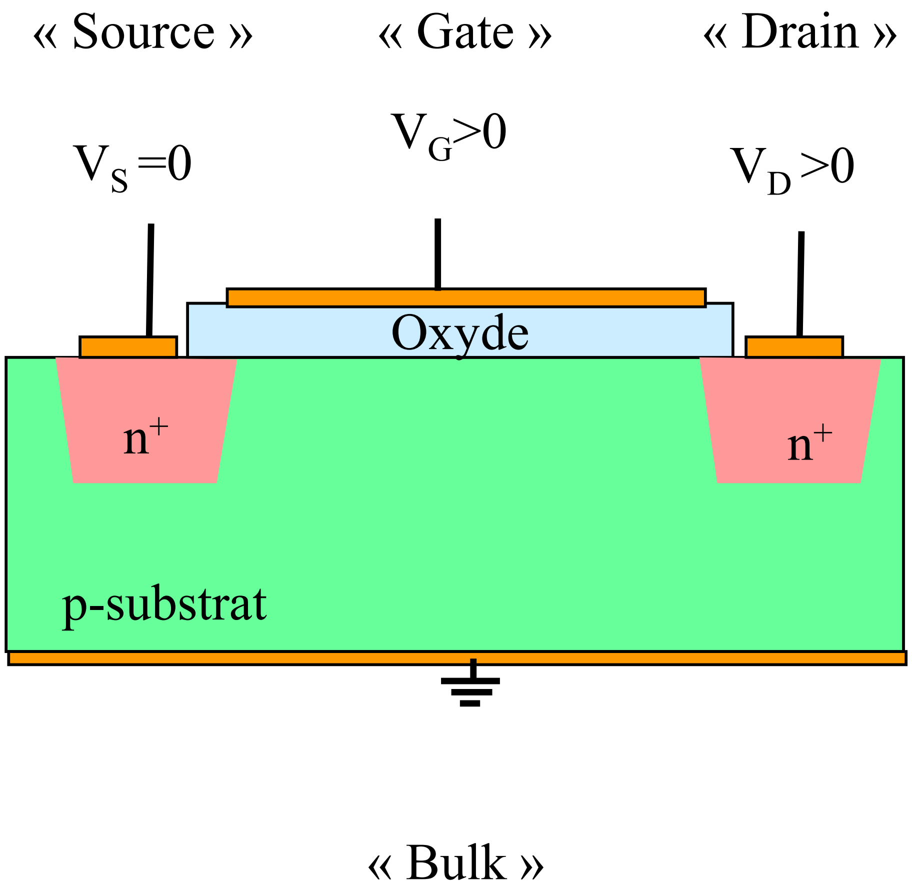
Exemple:
variation du threshold NMOS



$$V_{fb} + 2\psi_B \left(1 + 2\frac{C_{B,th}}{C_{ox}}\right)$$

Rappel: Structure MOSFET

NMOS: MOSFET à canal n



« Source »

« Gate »

« Drain »

$V_S = 0$

$V_G > 0$

$V_D > 0$

Oxyde

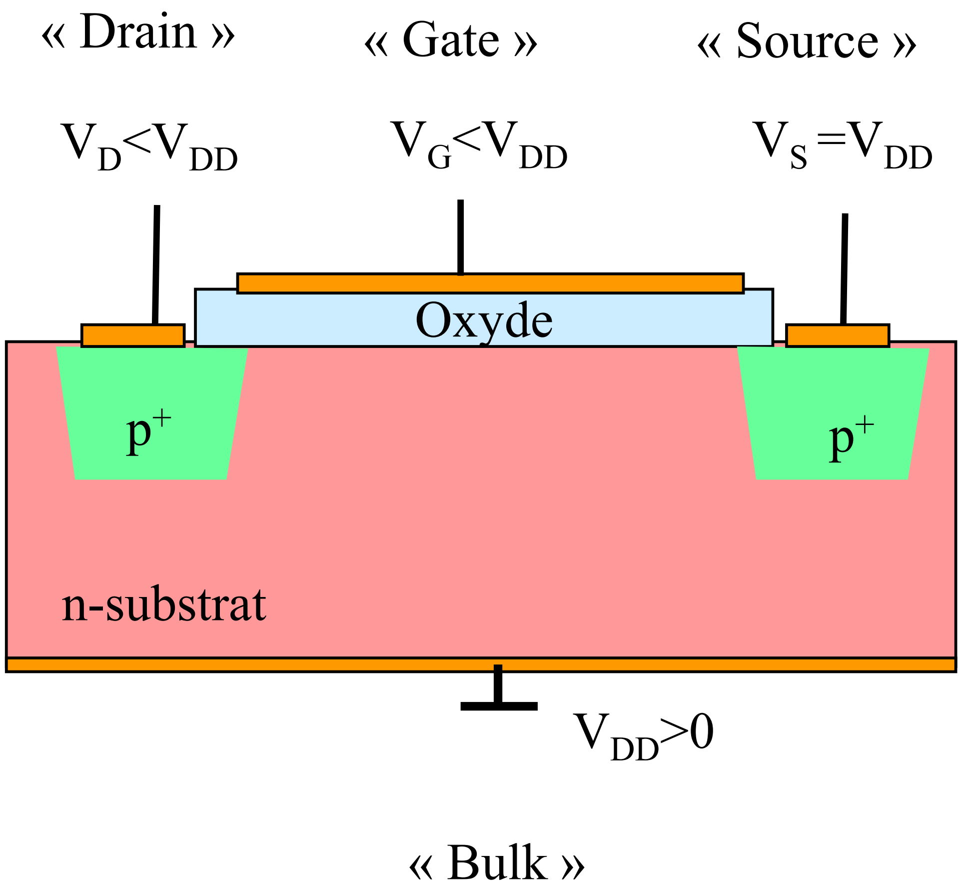
n^+

n^+

p-substrat

« Bulk »

PMOS: MOSFET à canal p



« Drain »

« Gate »

« Source »

$V_D < V_{DD}$

$V_G < V_{DD}$

$V_S = V_{DD}$

Oxyde

p^+

p^+

n-substrat

$V_{DD} > 0$

« Bulk »

PAB

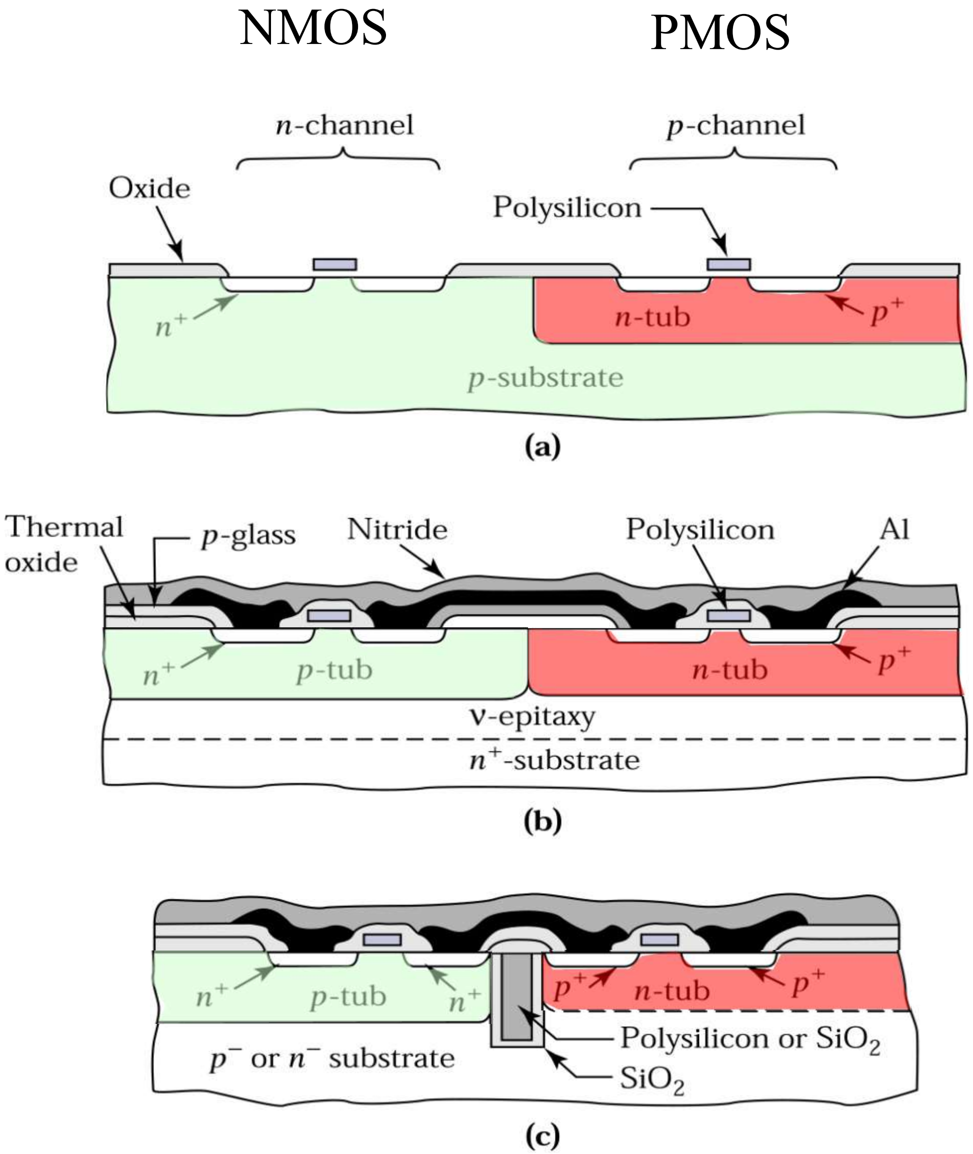
11.2: Complementary MOS: « CMOS »

Semiconductor Devices, 2/E by S. M. Sze

n-tub CMOS

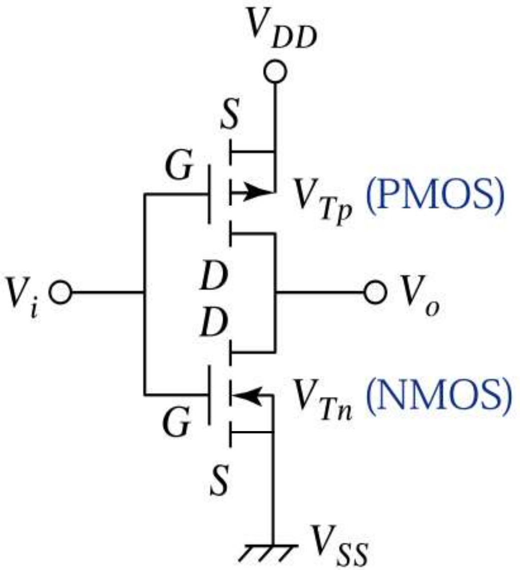
Twin-tub CMOS

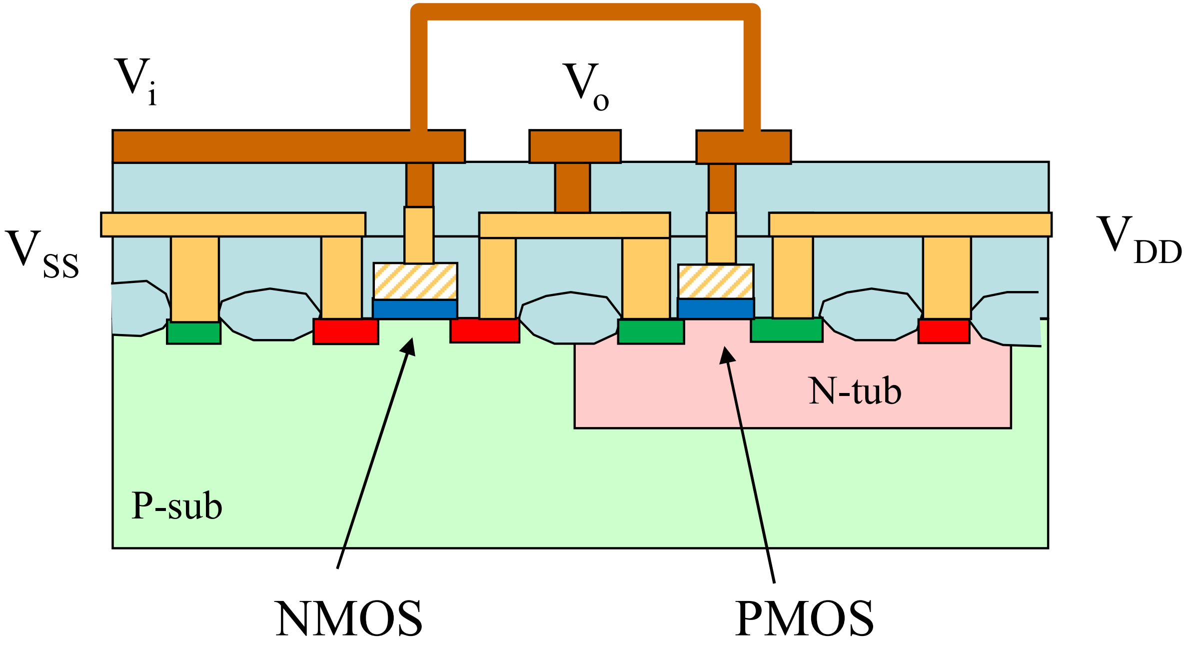
Refilled trenches CMOS



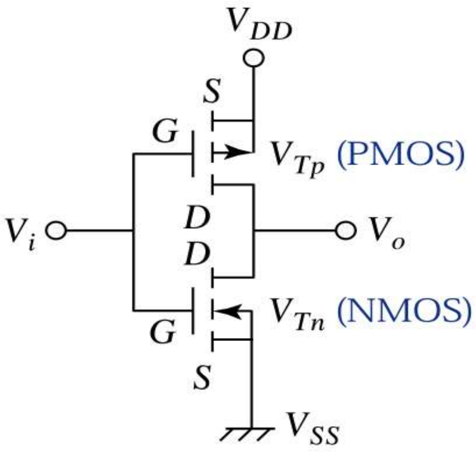
Inverseur CMOS: faible consommation

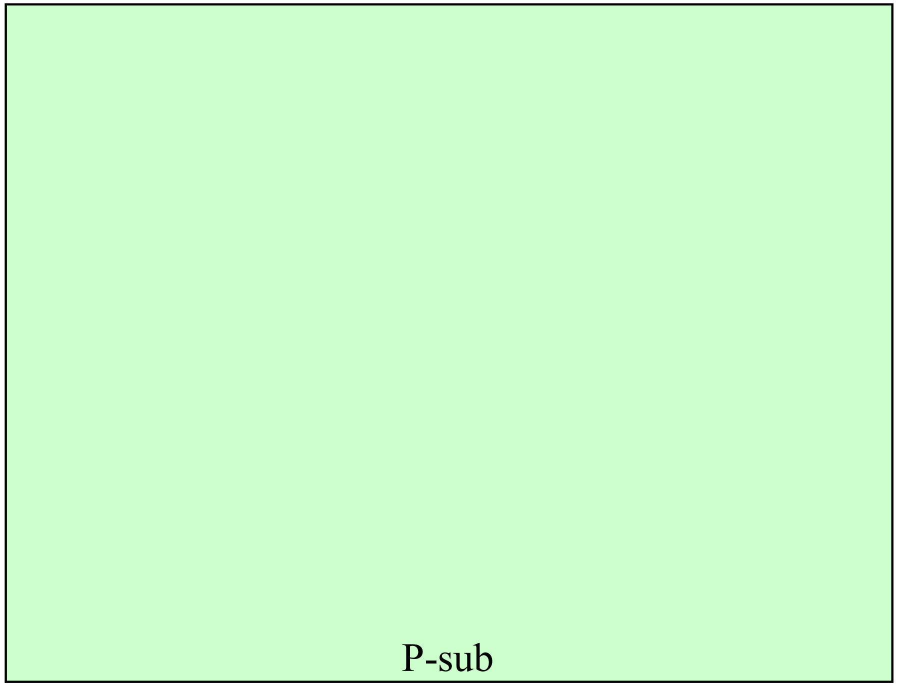
Semiconductor Devices, 2/E by S. M. Sze





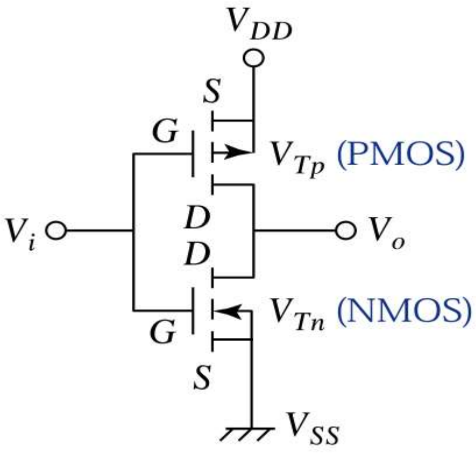
Techno CMOS (1)

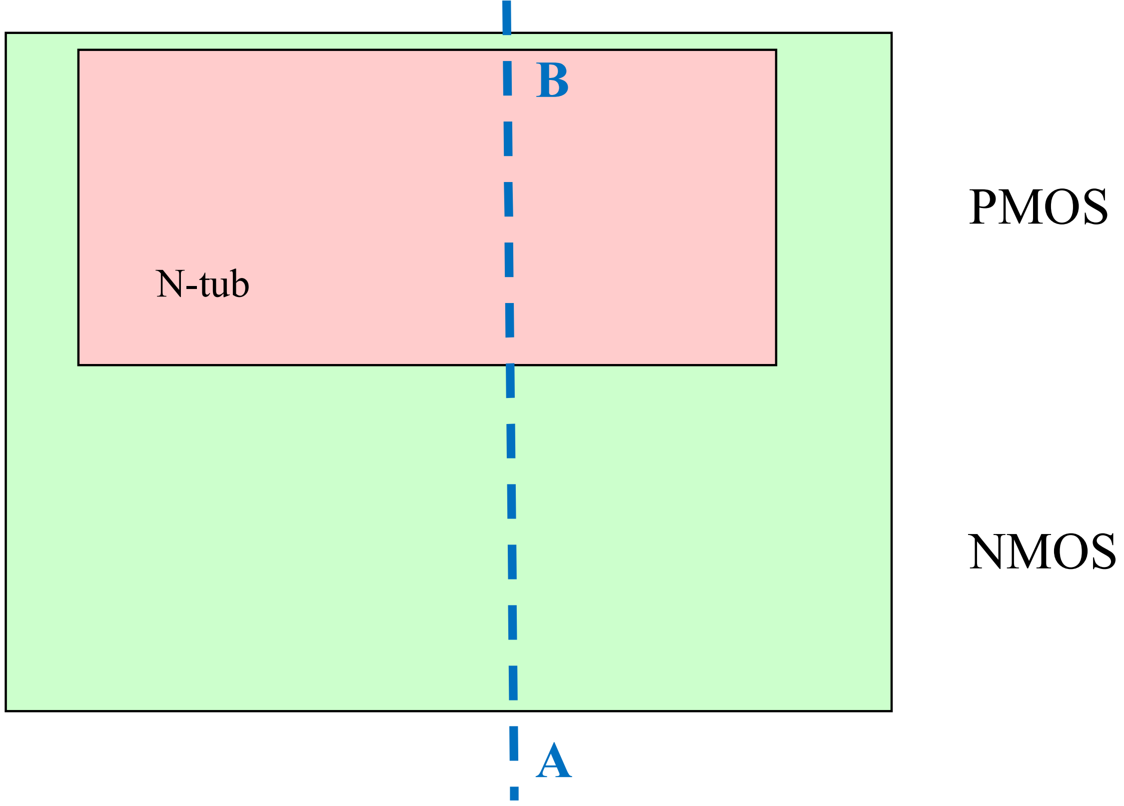




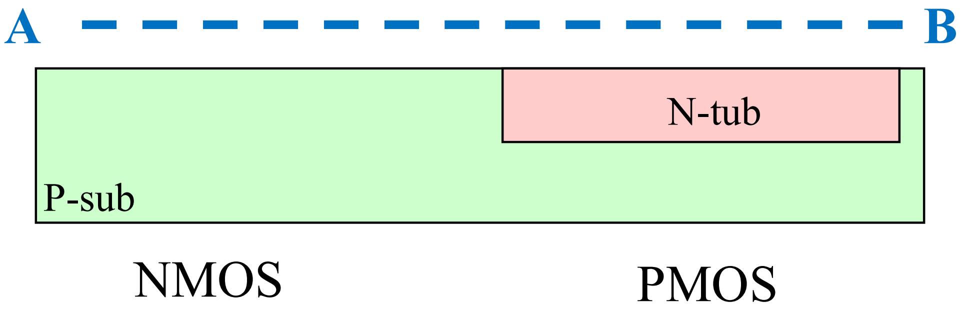
Start with p-substrat

Techno CMOS (2)

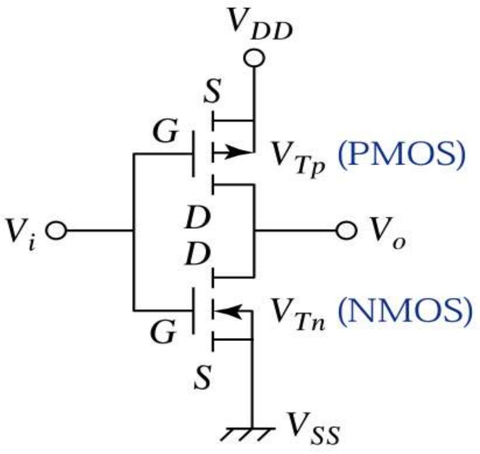


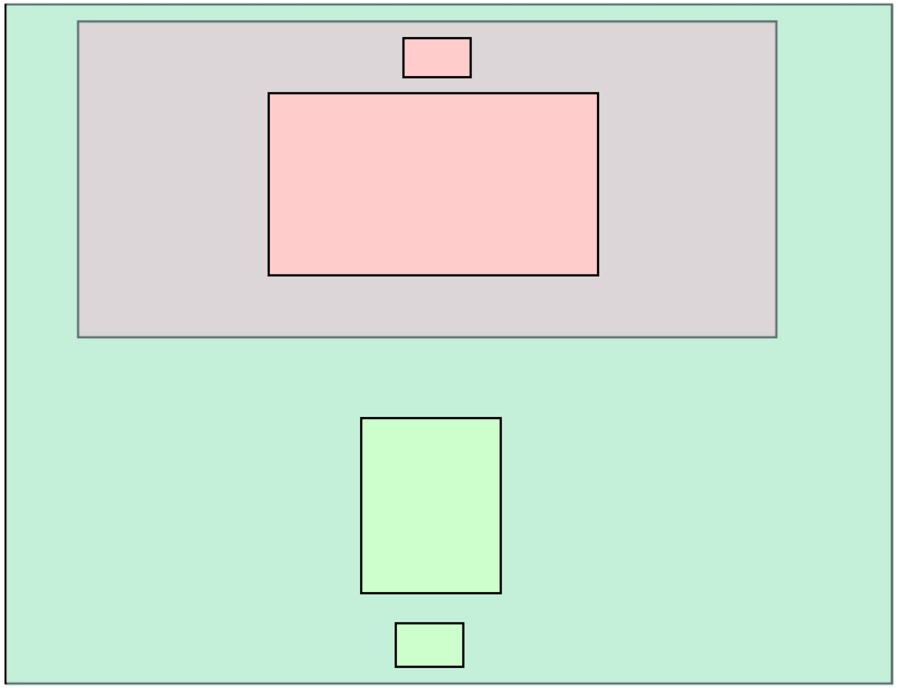


Step 1: N-tub
Mask 1: « Nwell »

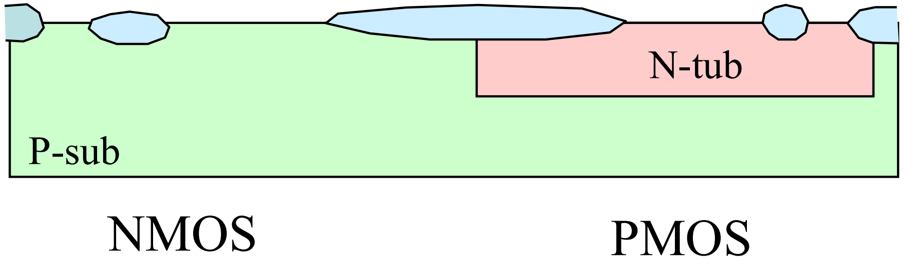


Techno CMOS (3)



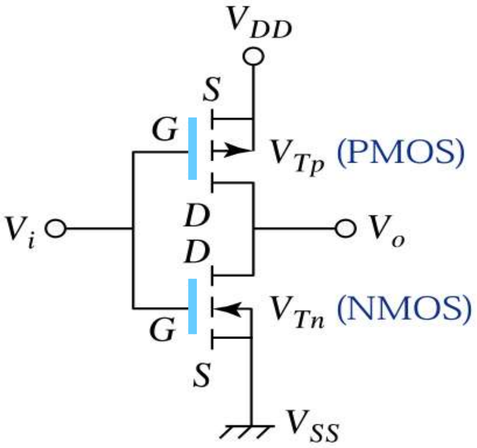


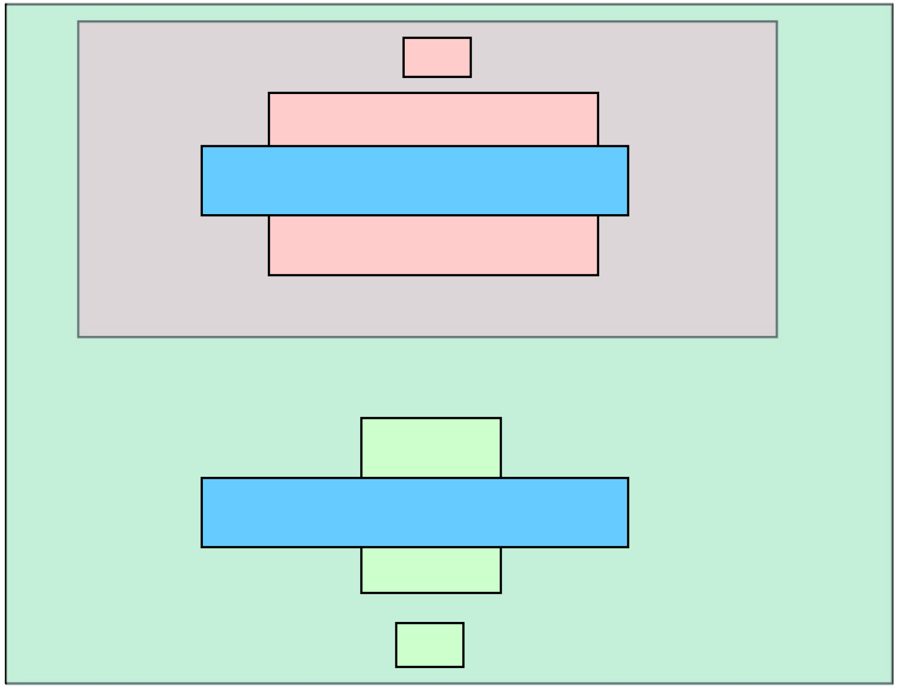
Step 2: Field oxyde
Mask 2: « active »



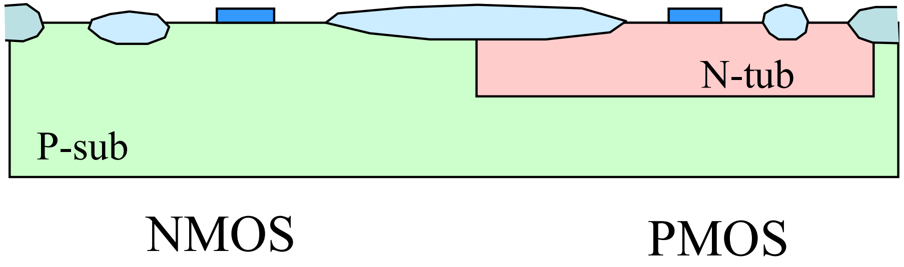
PAB

Techno CMOS (4)

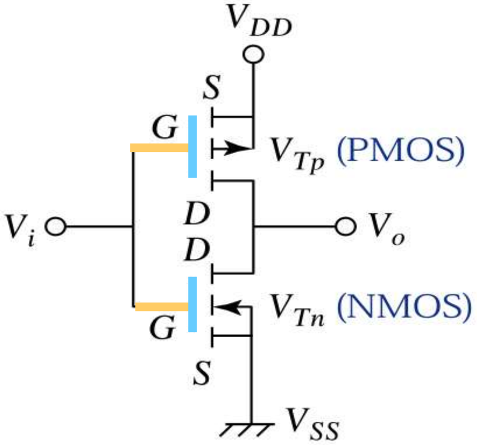


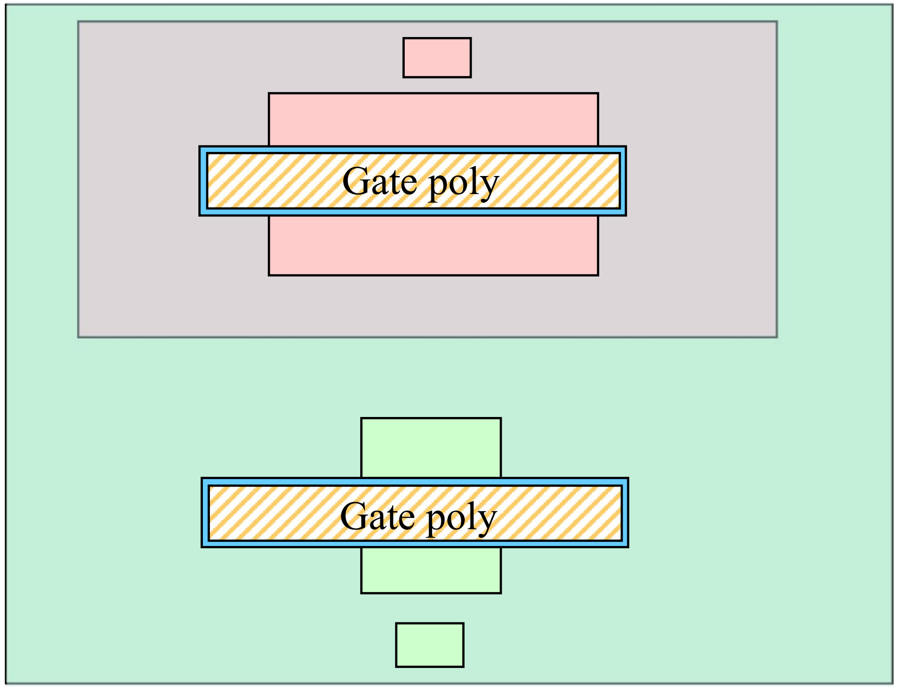


Step 3a: Gate oxyde
Mask 3: « Poly »

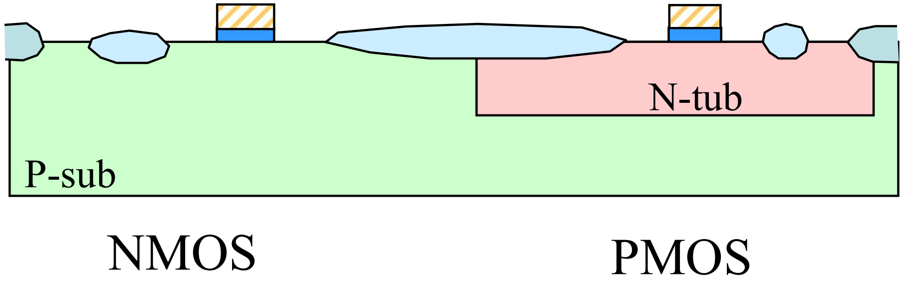


Techno CMOS (5)

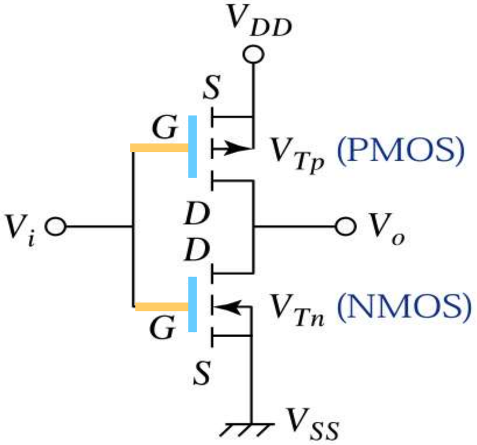


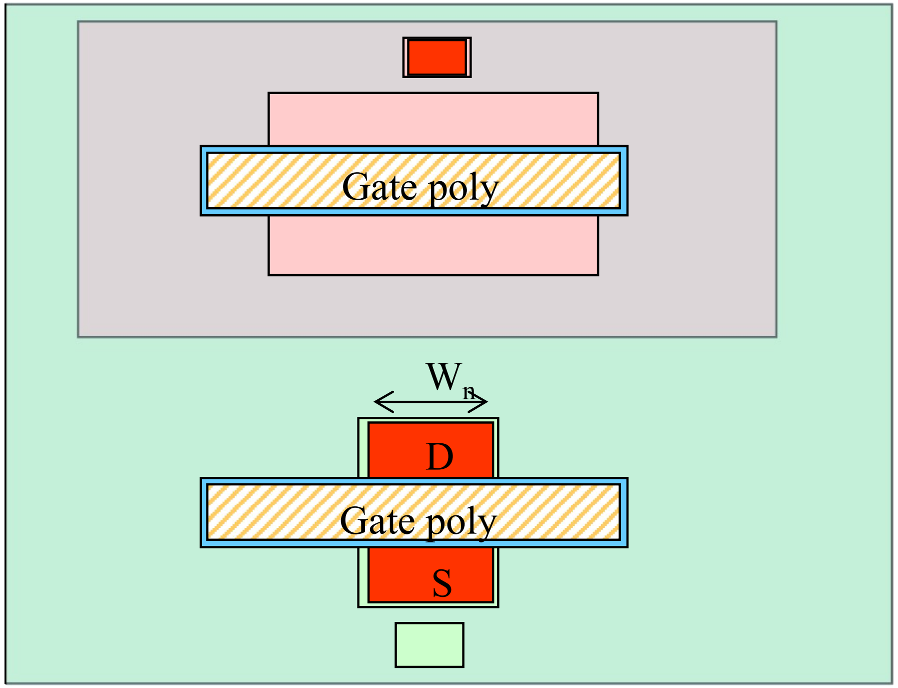


Step 3b: Gate poly
Mask 3: « Poly »

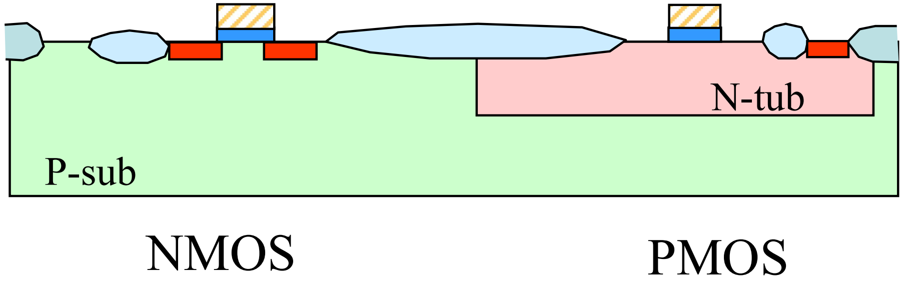


Techno CMOS (6)

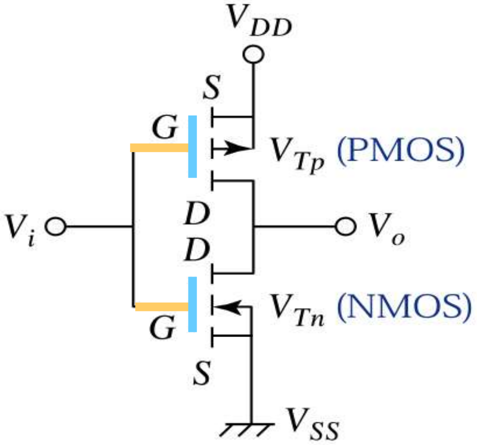


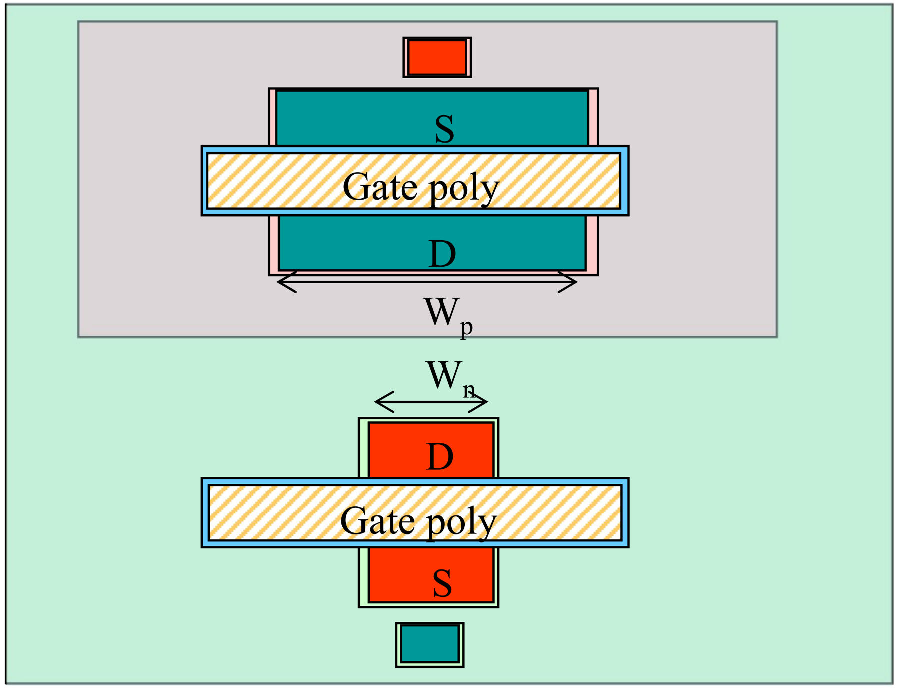


Step 4: N+ contacts
Mask 4: « Nselect »

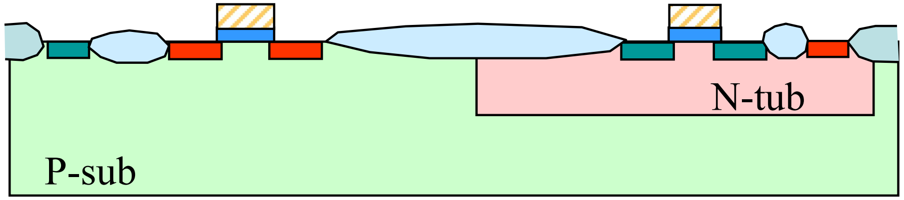


Techno CMOS (7)



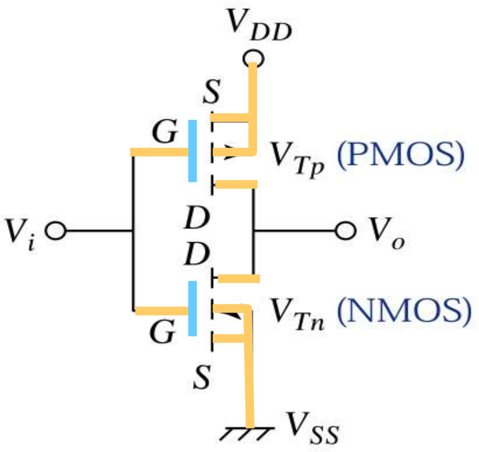


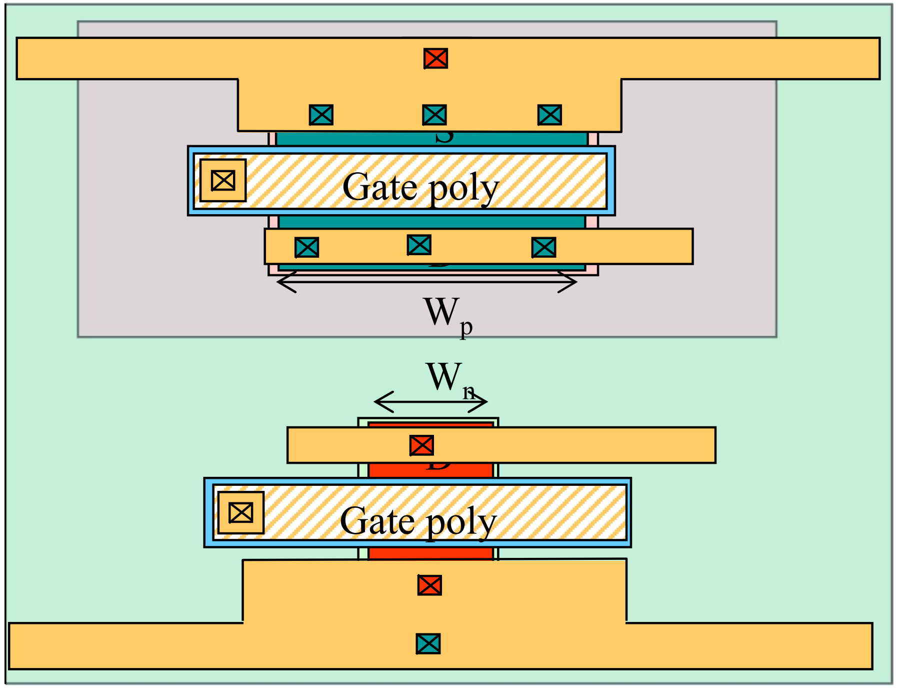
Step 5: P+ contacts
Mask 5: « Pselect »



NMOS PMOS

Techno CMOS (8)

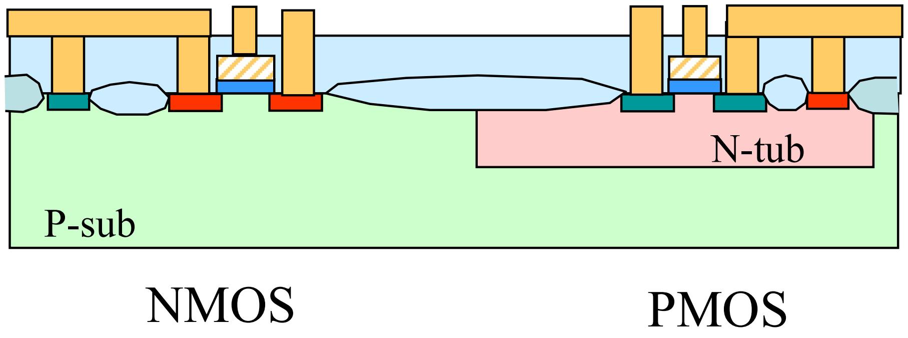




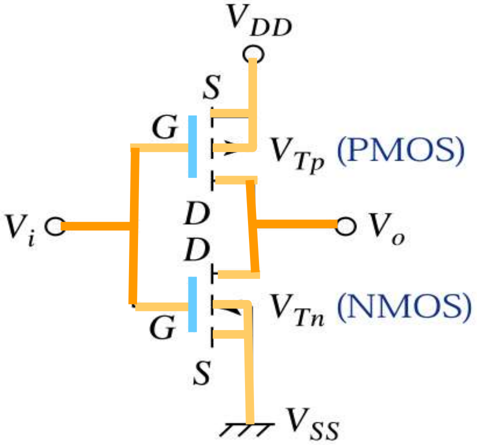
Step 6-7: Contact + metal 1

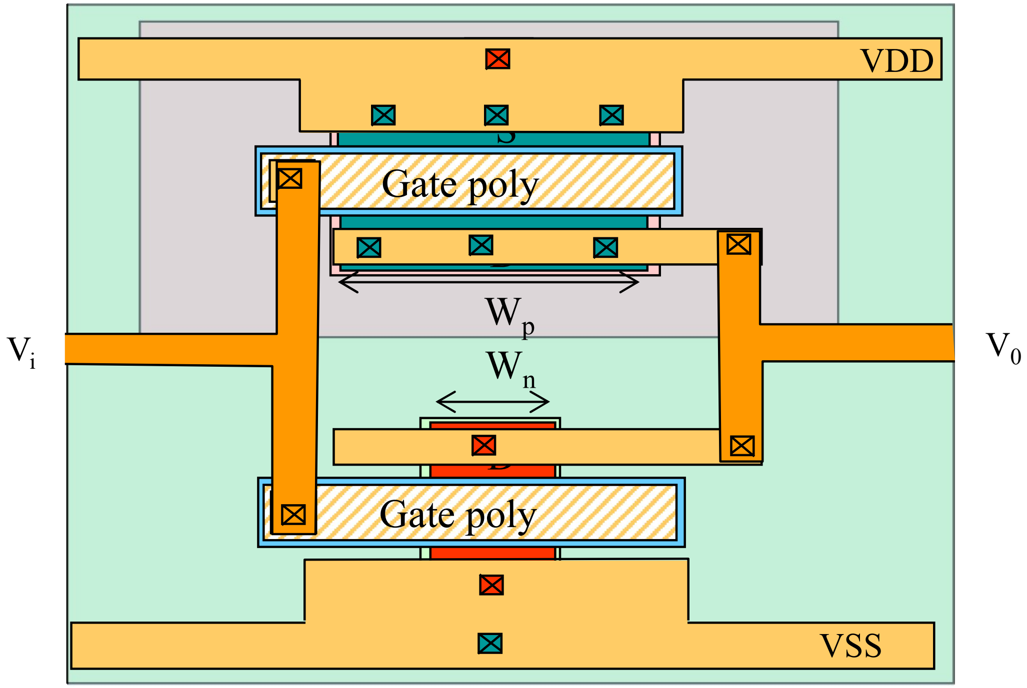
Mask 6: « Contact»

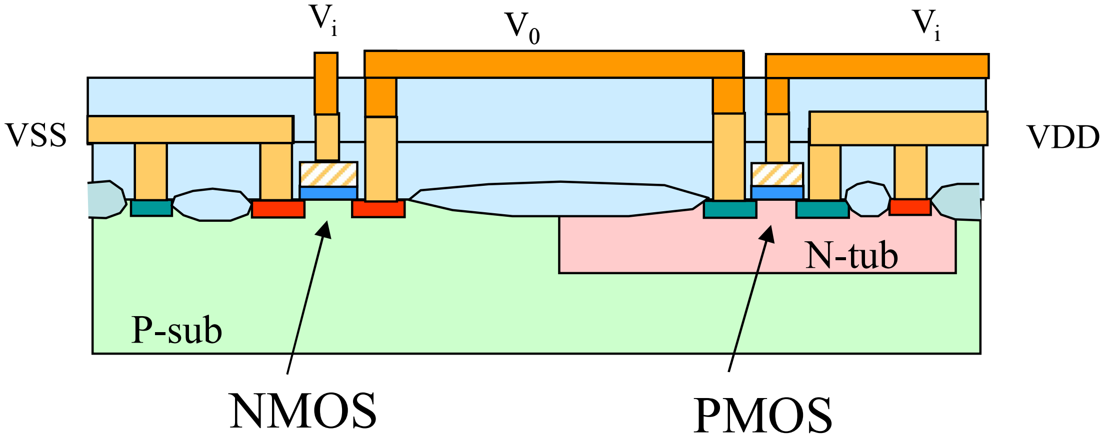
Mask 7: « Metal 1 »



Techno CMOS (9)







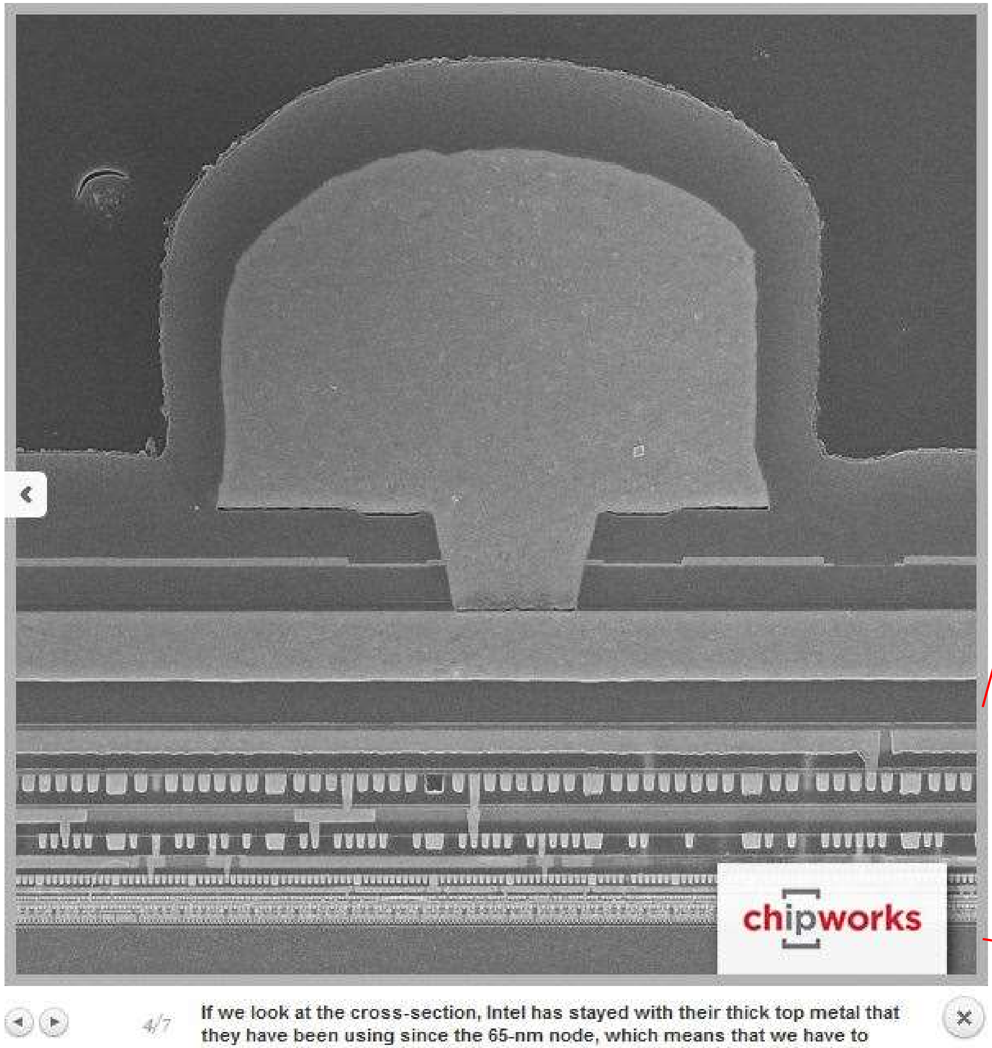
Step 8-9: Via et metal 2

Mask 8: « Via »

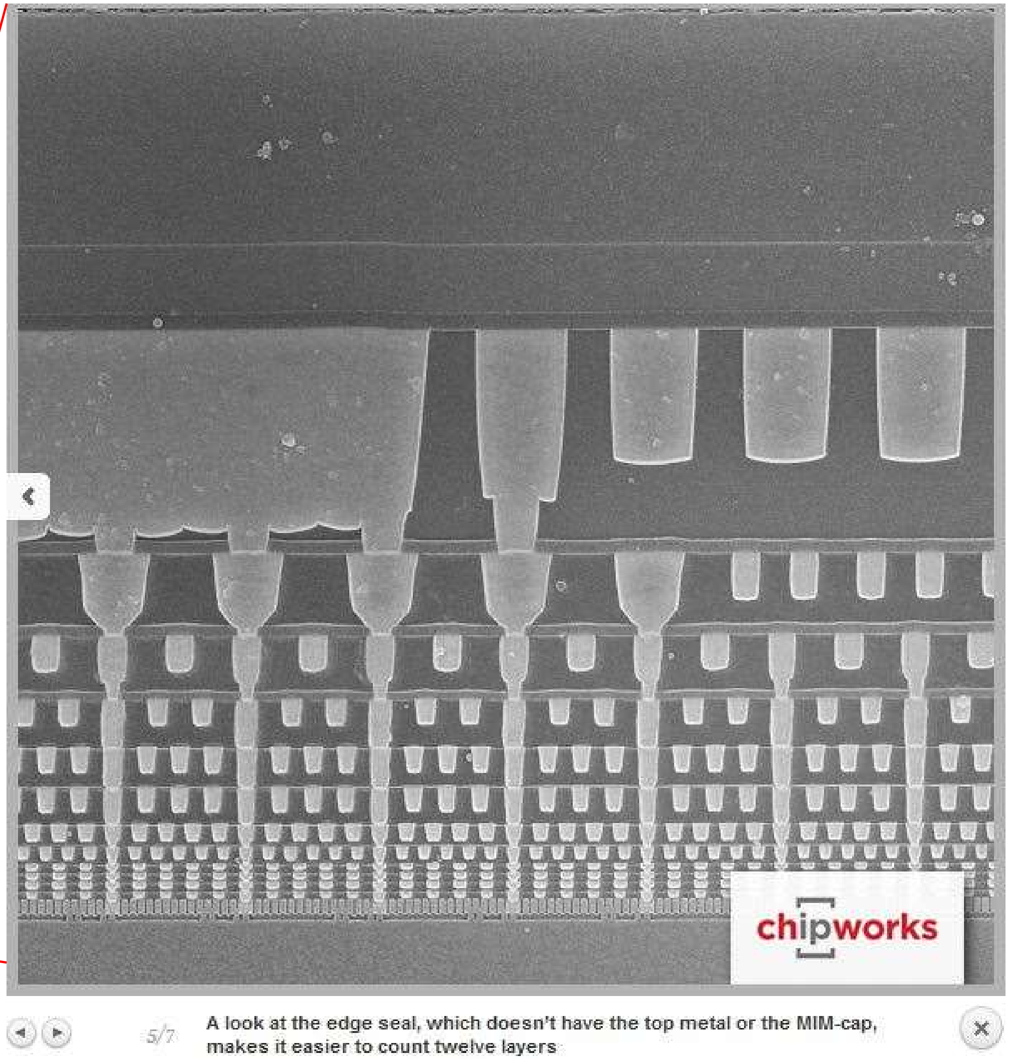
Mask 9: « Metal 2 »

Métallisations: Intel 2014: 13 layers

http://www.chipworks.com/en/technical-competitive-analysis/resources/blog/intels-14-nm-parts-are-finally-here/



If we look at the cross-section, Intel has stayed with their thick top metal that they have been using since the 65-nm node, which means that we have to squint awfully hard to see THIRTEEN layers of metal, and a MIM-cap layer under the top metal.

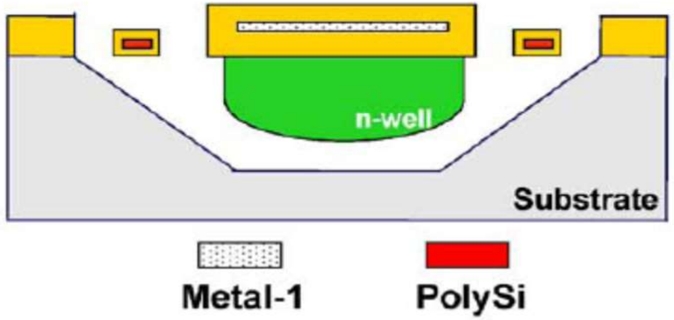


A look at the edge seal, which doesn't have the top metal or the MIM-cap, makes it easier to count twelve layers

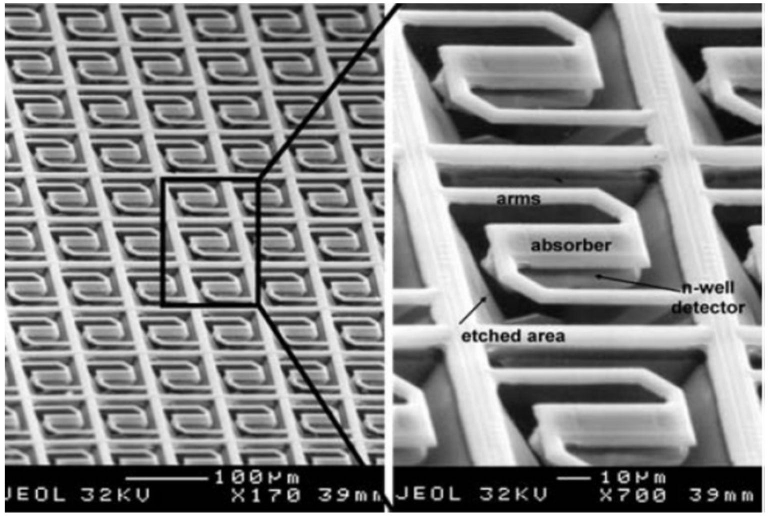
FinFET structures, 14nm gates

Example: bulk-micromachining

IR camera (room temperature)
Array of silicon bolometers

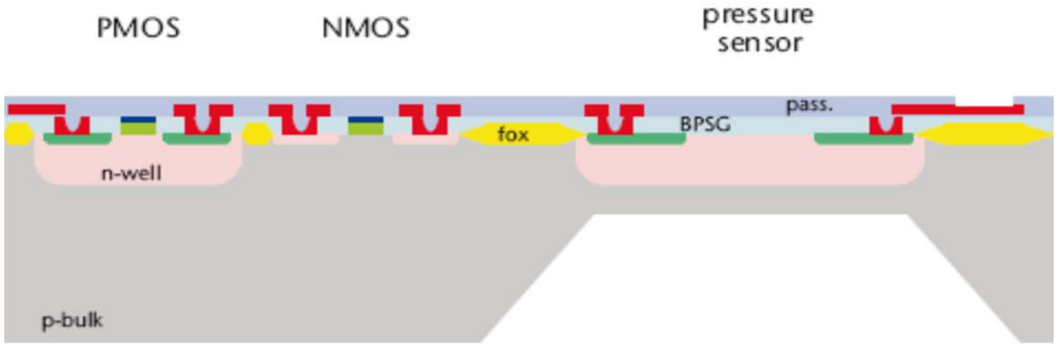


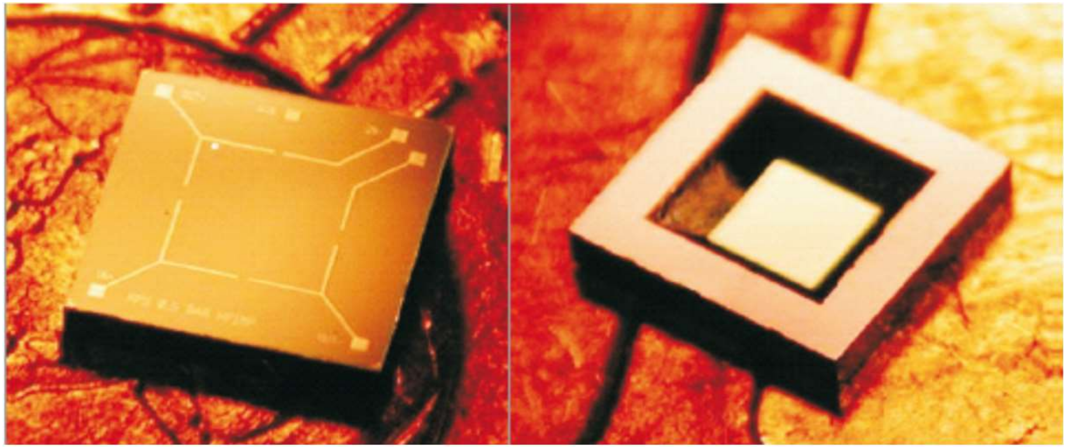
S. Erminoglu et al.



T. Akin

X-Fab facilities

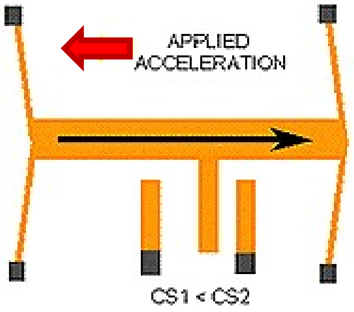


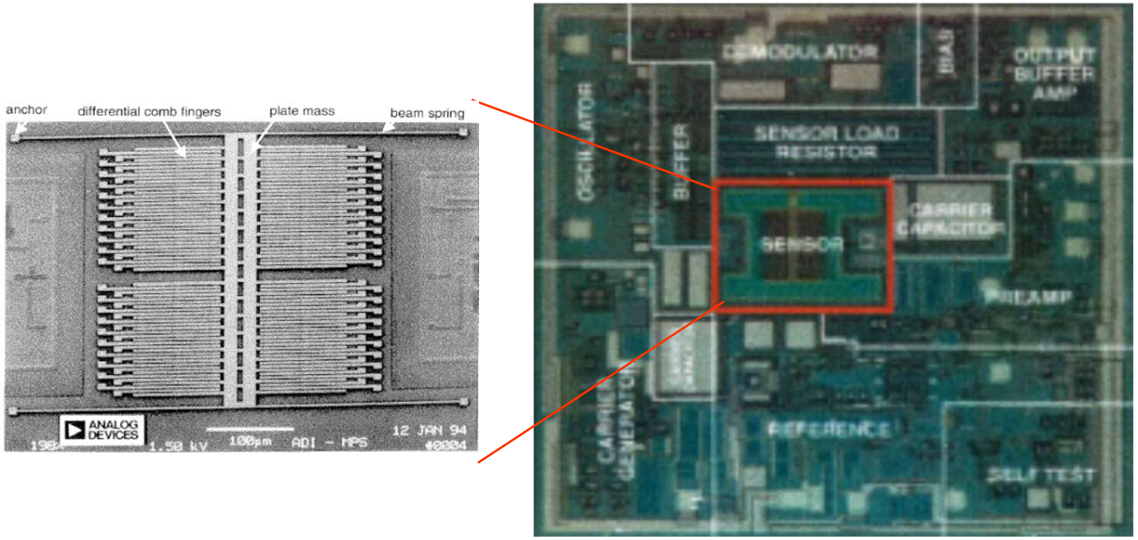


XC10 CMOS process

Example: surface micromachining

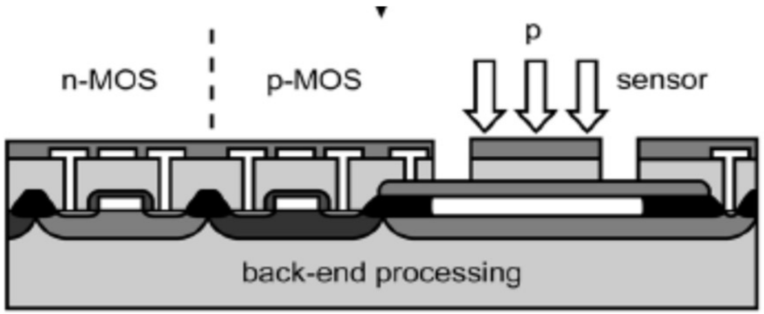
Accelerometer (Analog Devices)

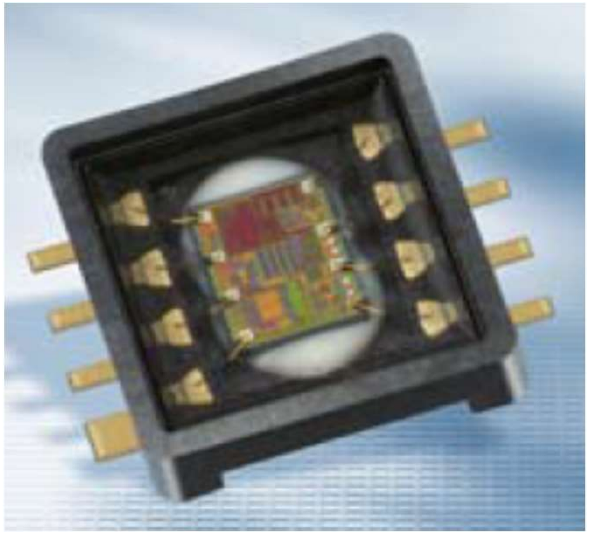




ADXL 50-series

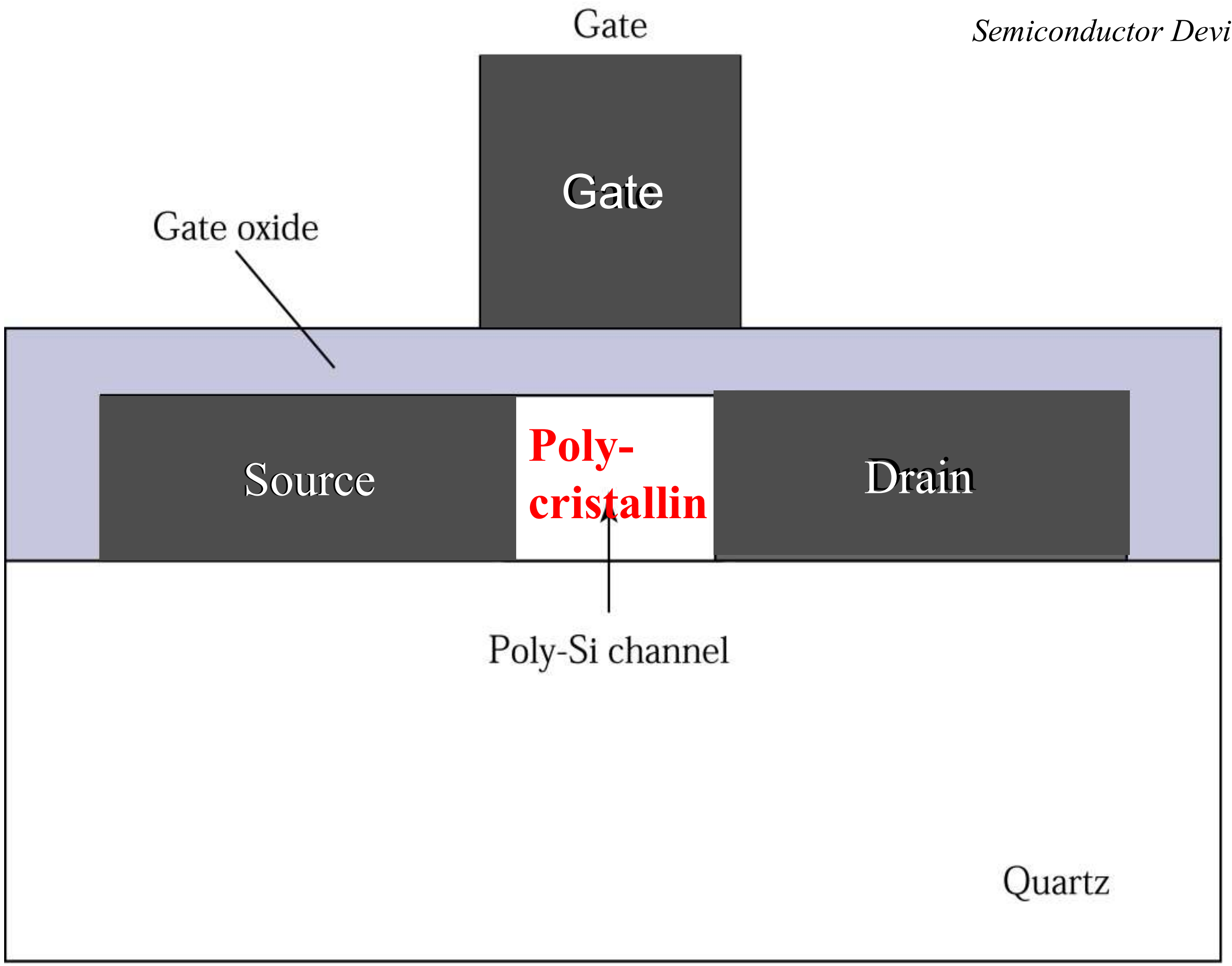
Pressure sensor (Infineon)





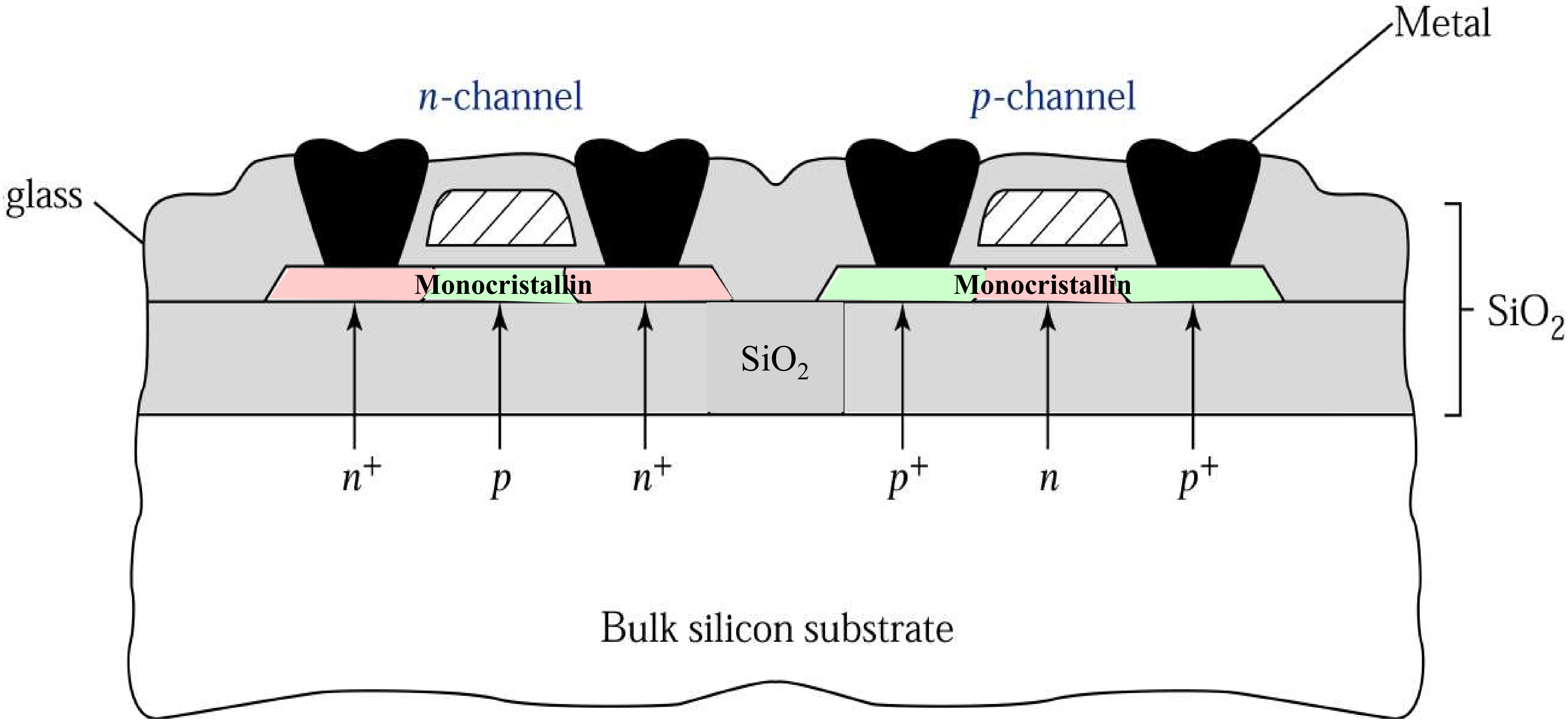
KP-series

11.3: Polysilicon TFT



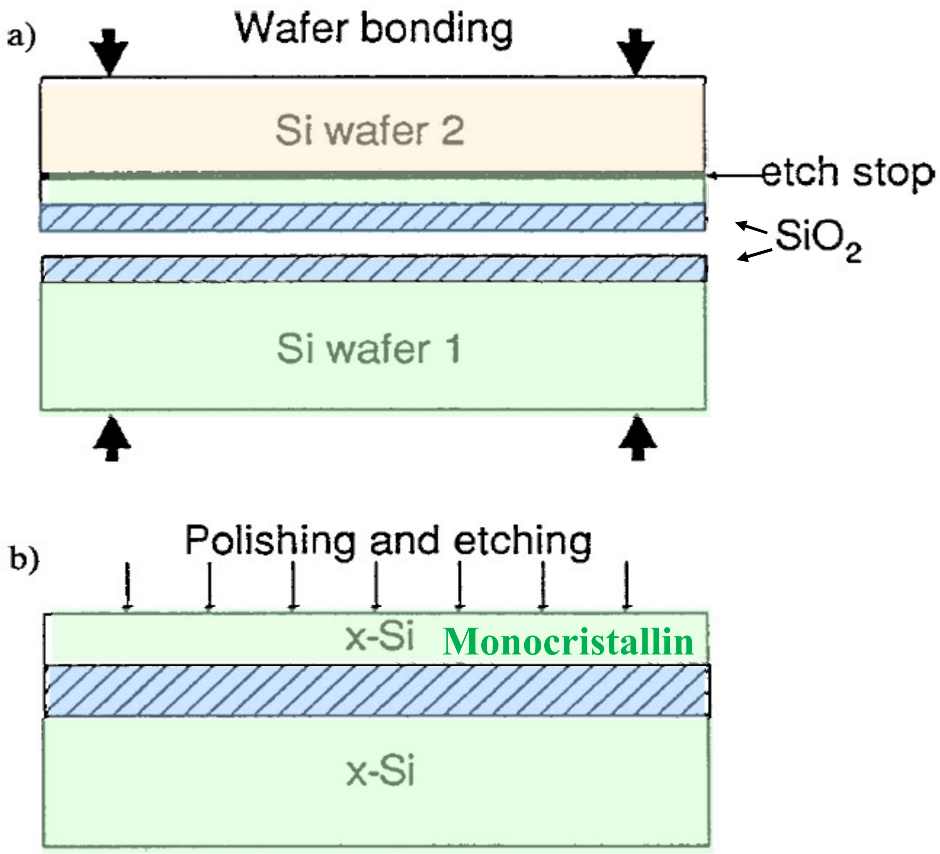
Semiconductor Devices, 2/E by S. M. Sze

Silicon-On-Isolator (SOI)



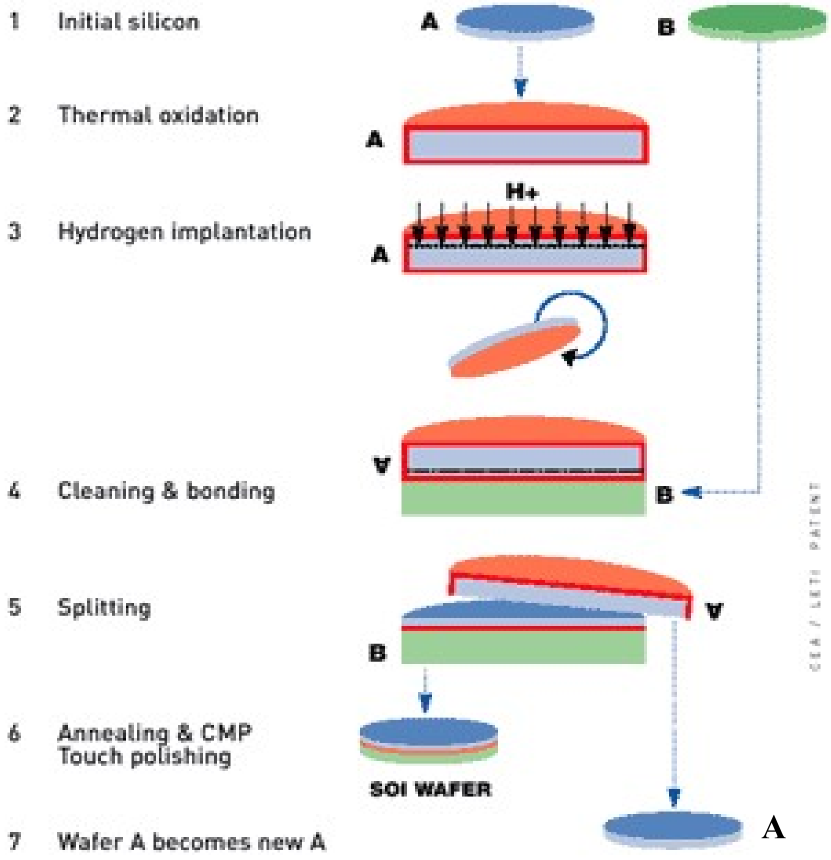
Silicon On Isolator (SOI)

Bond-and-Etchback SOI (BESOI)



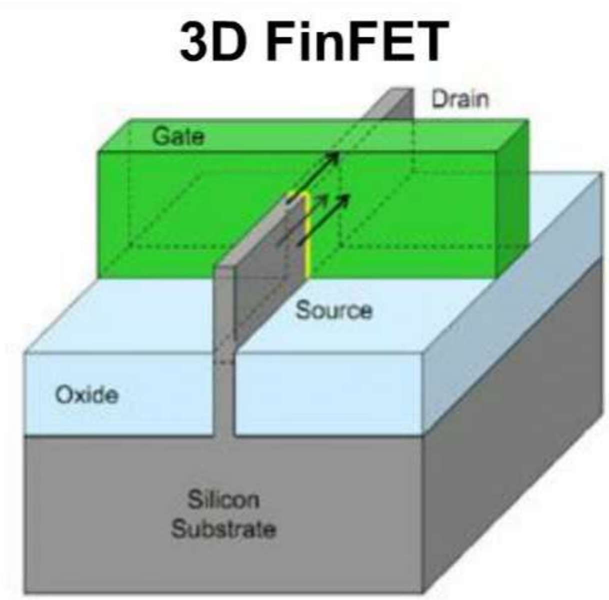
G.K. Celler et al., J. Àppl. Phys., Vol. 93, 2003, 4955-4978

SmartCut^{TM}



SOITEC SÀ

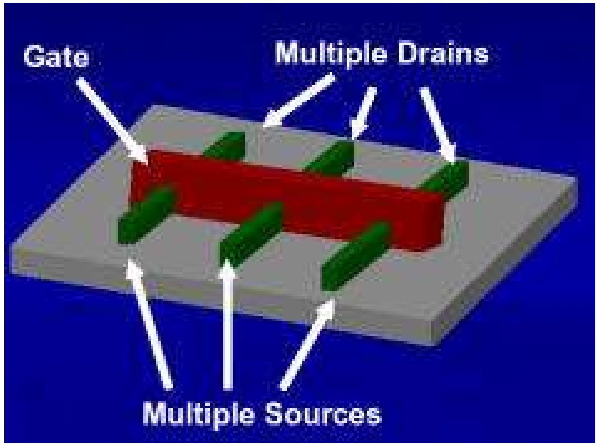
Intel Tri-gate «FinFET»:
14nm gate (2014)



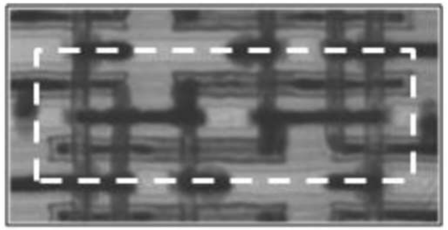
3-D Tri-Gate transistor form conducting channels on three sides of a vertical fin structure, providing "fully depleted" operation

https://www.semiwiki.com/forum/content/1908-finfet-process-modeling-extraction-16-nm-below.html

http://en.wikipedia.org/wiki/Multigate_device

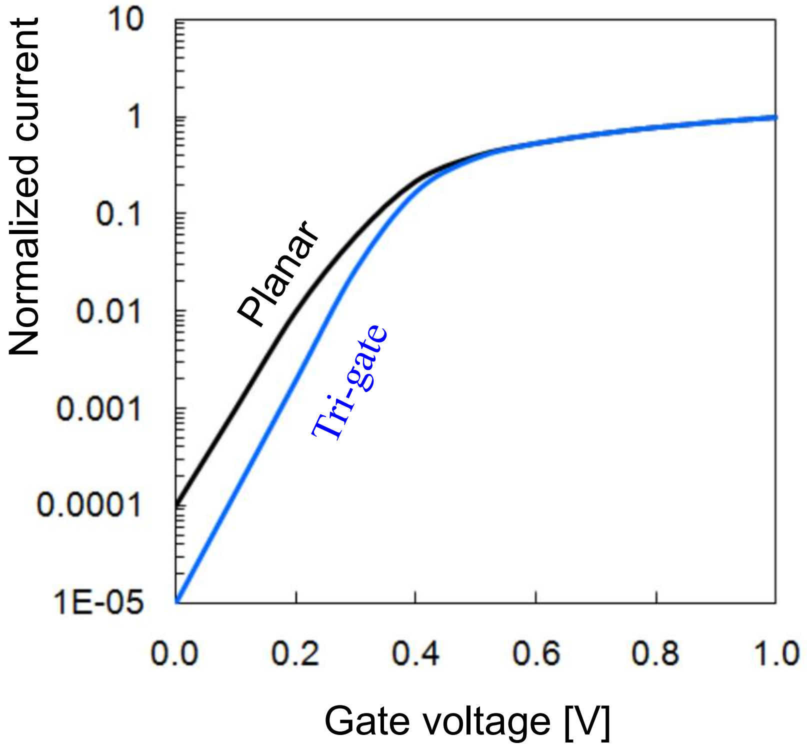


SRAM memory



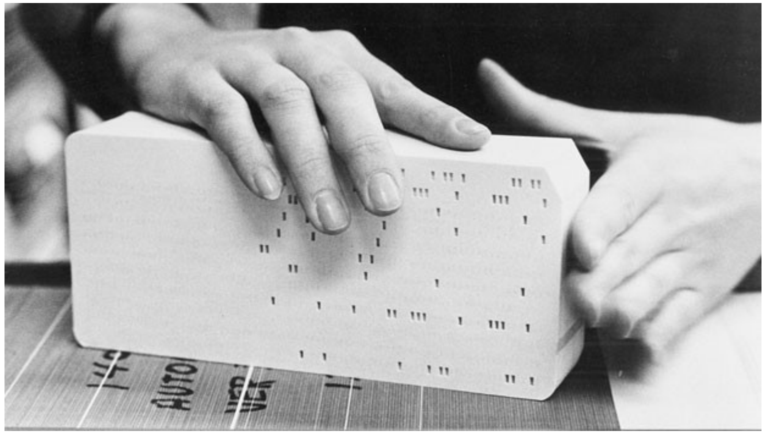
.0588 um^2 = 430 nm x 135 nm

M. Bohr «Intel's Revolutionary 22 nm Transistor Technology», INTEL May 2011



http://download.intel.com/newsroom/kits/14nm/pdfs/Intel_14nm_New_uArch.pdf

11.6 Mémoires



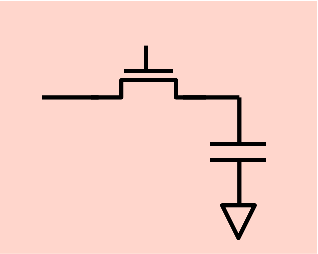
Mémoires électroniques: vue d'ensemble

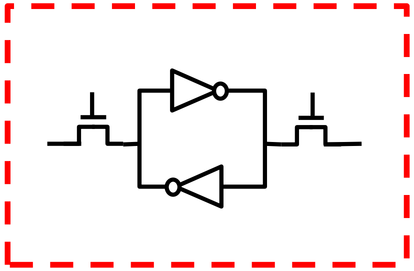
Semiconductor Memories

Volatile

Read/Write (R/W) Memory
or Random Access Memory (RAM)

- Dynamic RAM (DRAM)
- Static RAM (SRAM)

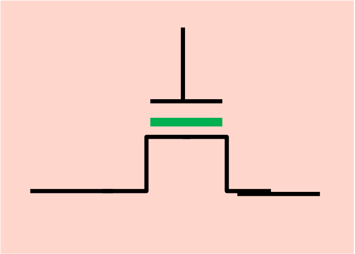




Non-volatile

Read-Only Memory (ROM)

- Mask (Fuse) ROM
- Programmable ROM (PROM)
  - Erasable PROM (EPROM)
  - Electrically Erasable PROM (EEPROM)
- Flash Memory
- Ferroelectric RAM (FRAM)

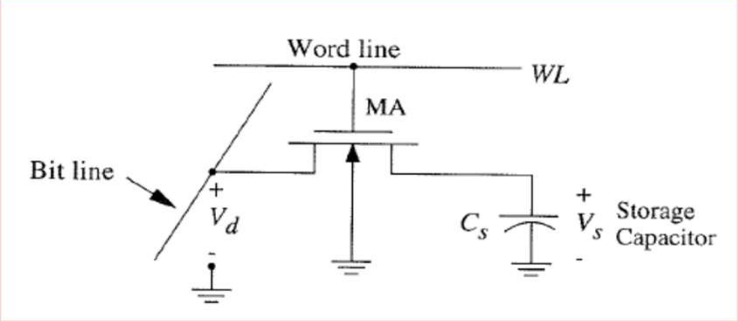


S.M. Kang, Y. Leblebici, "CMOS digital integrated circuits: analysis and design", McGraw-Hill

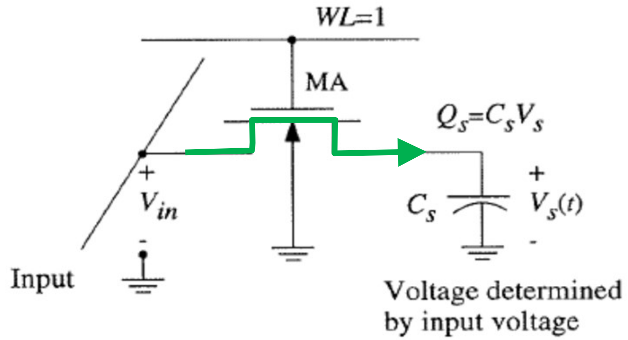
Volatile memories: DRAM

Capacity with single transistor

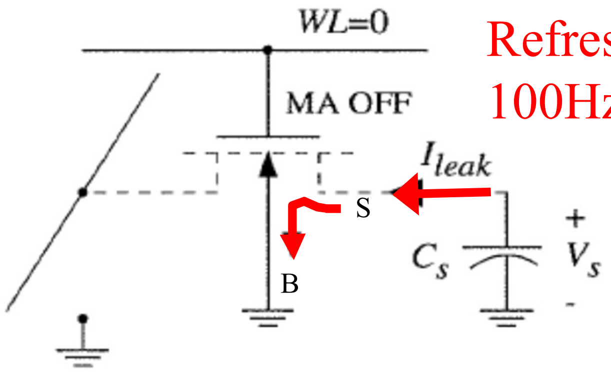
Schéma de base DRAM



Écriture dans une DRAM

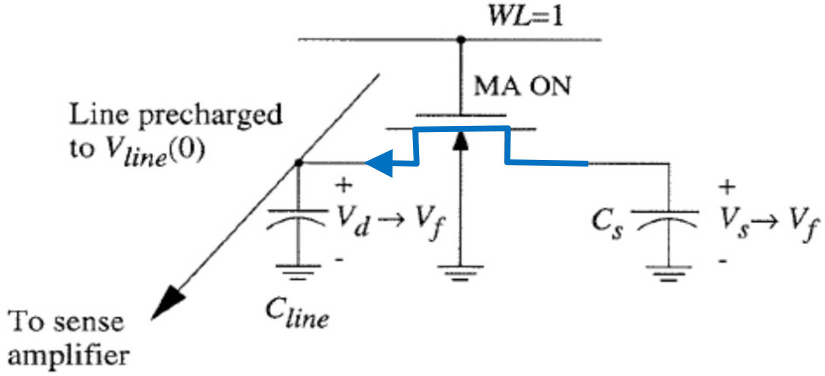


Retenue dans une DRAM



Refreshed:
100Hz

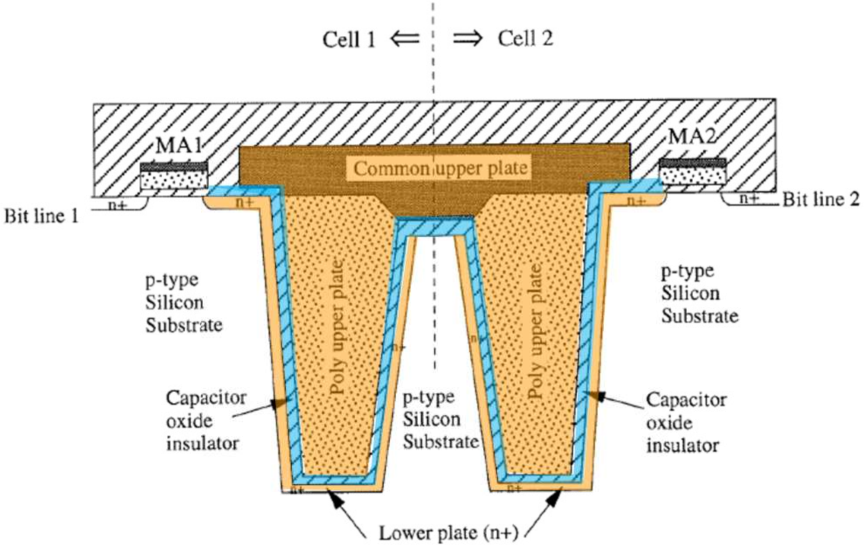
Lecture et effacement d’une DRAM

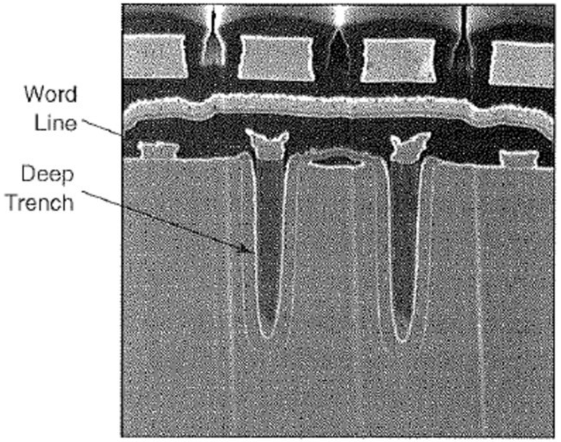


J.P. Uyemura “CMOS logic circuit design”, Kluwer Academic Publishers

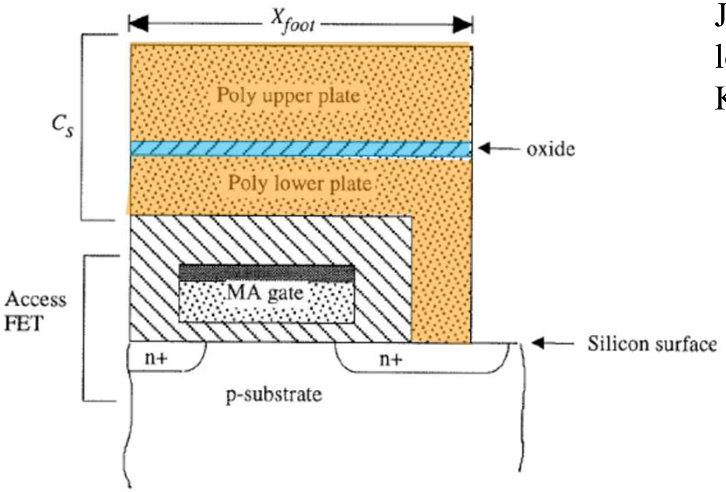
Volatile memories: DRAM

Trench capacitor DRAM

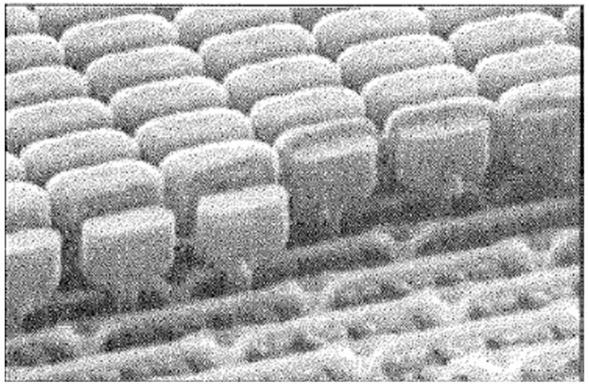




Stacked capacitor DRAM



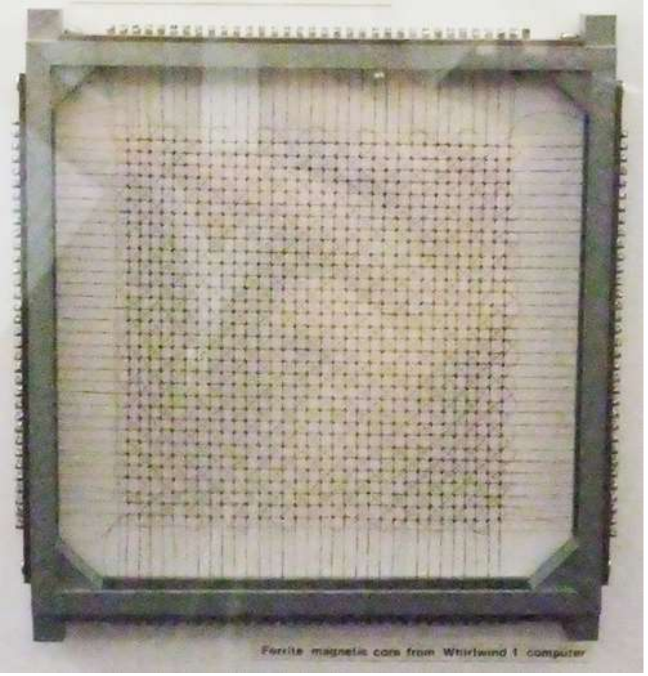
J.P. Uyemura “CMOS logic circuit design”, Kluwer Academic Publishers



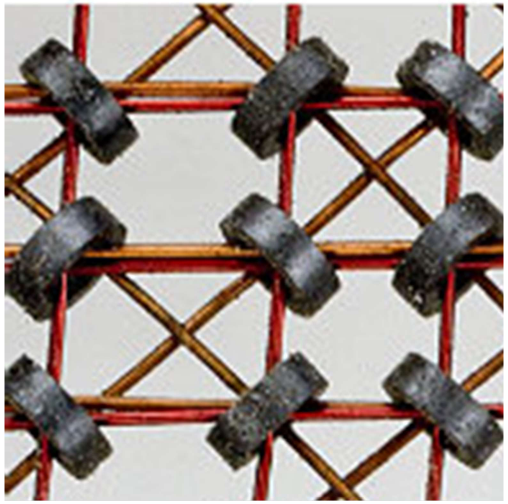
S.M. Kang, Y. Leblebici, “CMOS digital integrated circuits: analysis and design”, McGraw-Hill

Mémoires non-volatiles
Historique: magnetic core memory

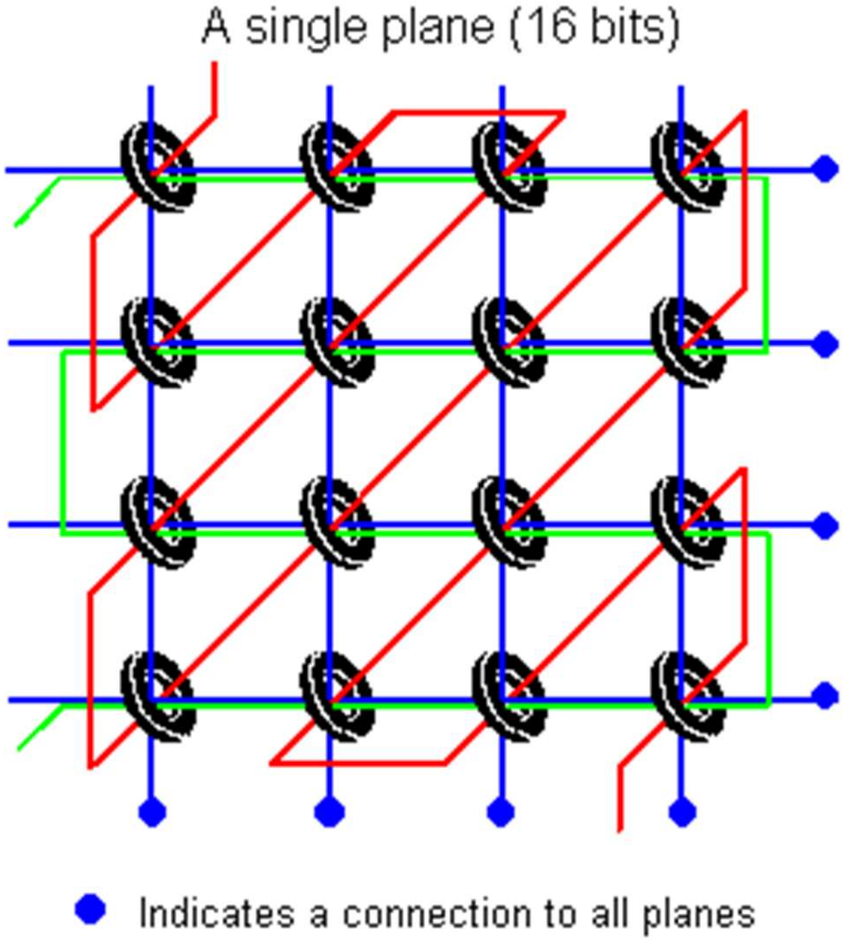
Magnetic core memory
Whirlwind 1 computer 1953
London, Science Museum.



1024 binary digits per plane
(16 planes in computer)



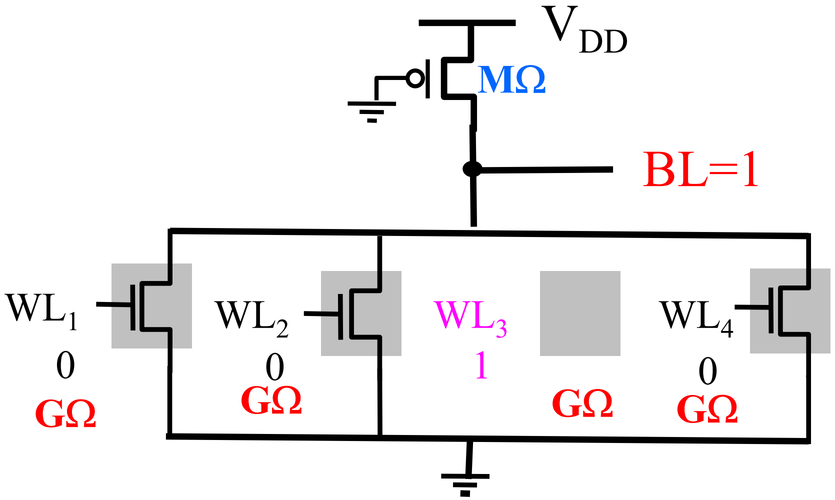
http://www.hpmuseum.org/tech9100.htm

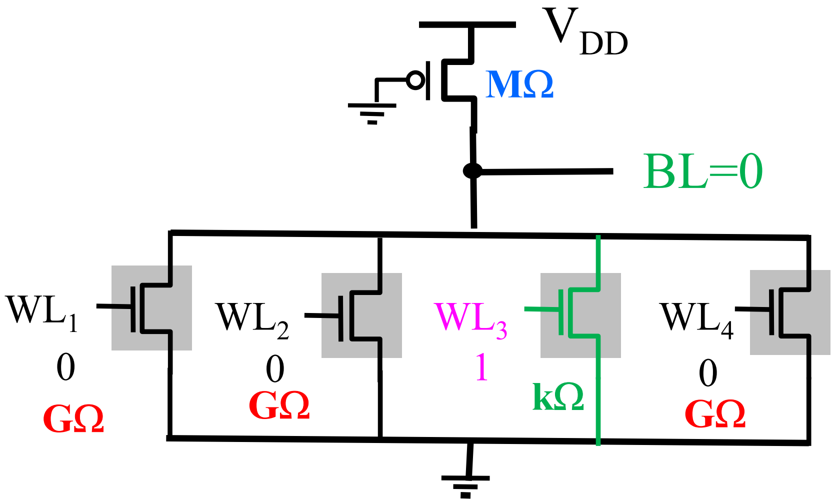


http://www.computerhistory.org/revolution/memory-storage/8/253

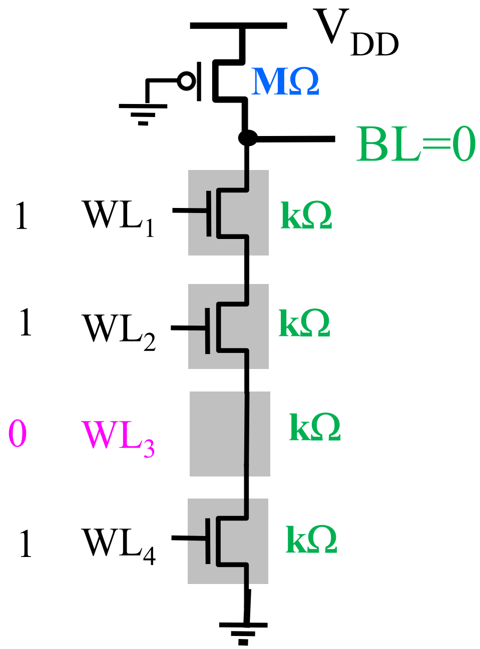
Configurations

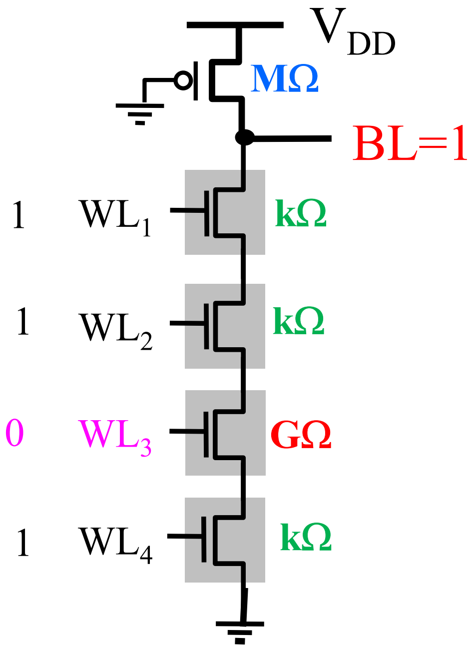
«NOR»: NMOS en parallèle



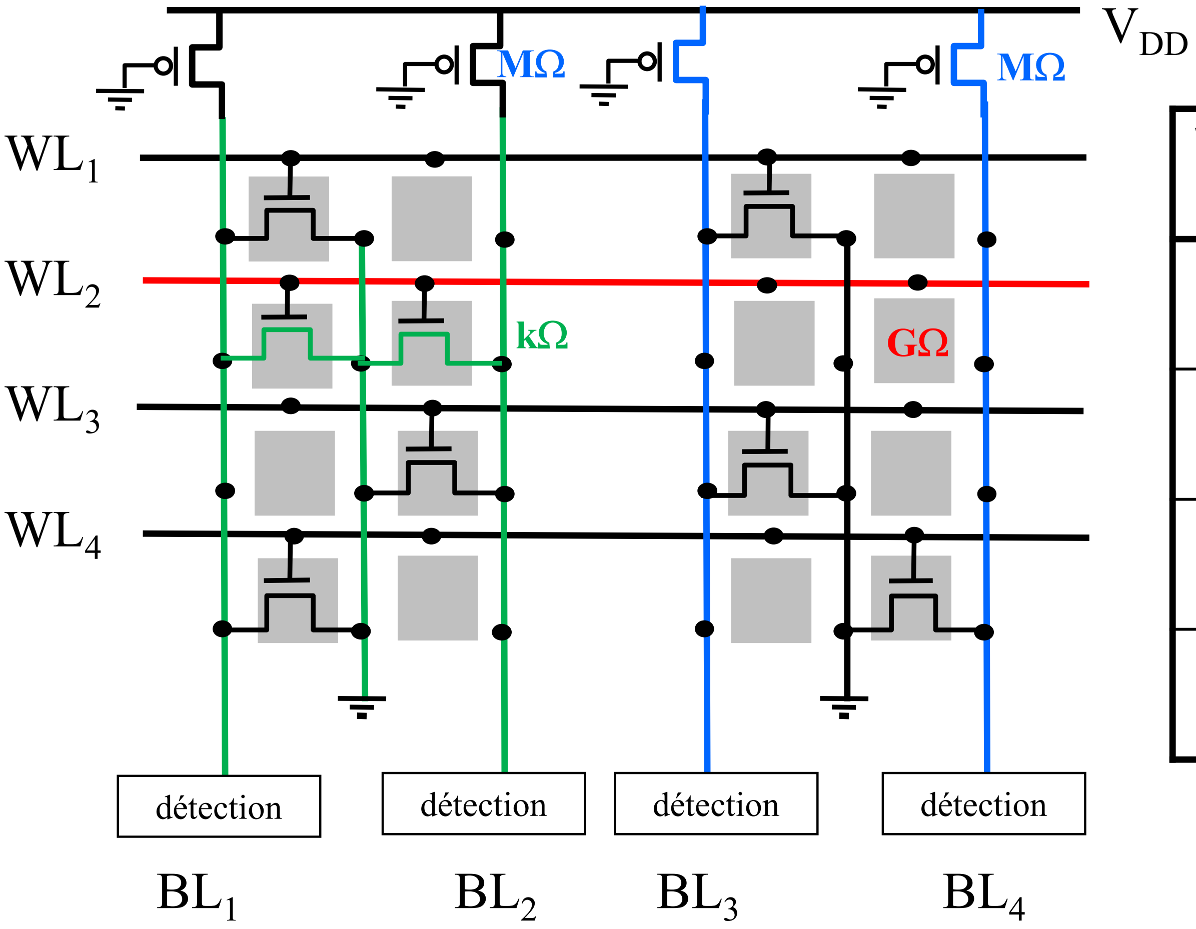


«NAND»: NMOS en série





Mémoires non-volatiles:
ROM en configuration “NOR”

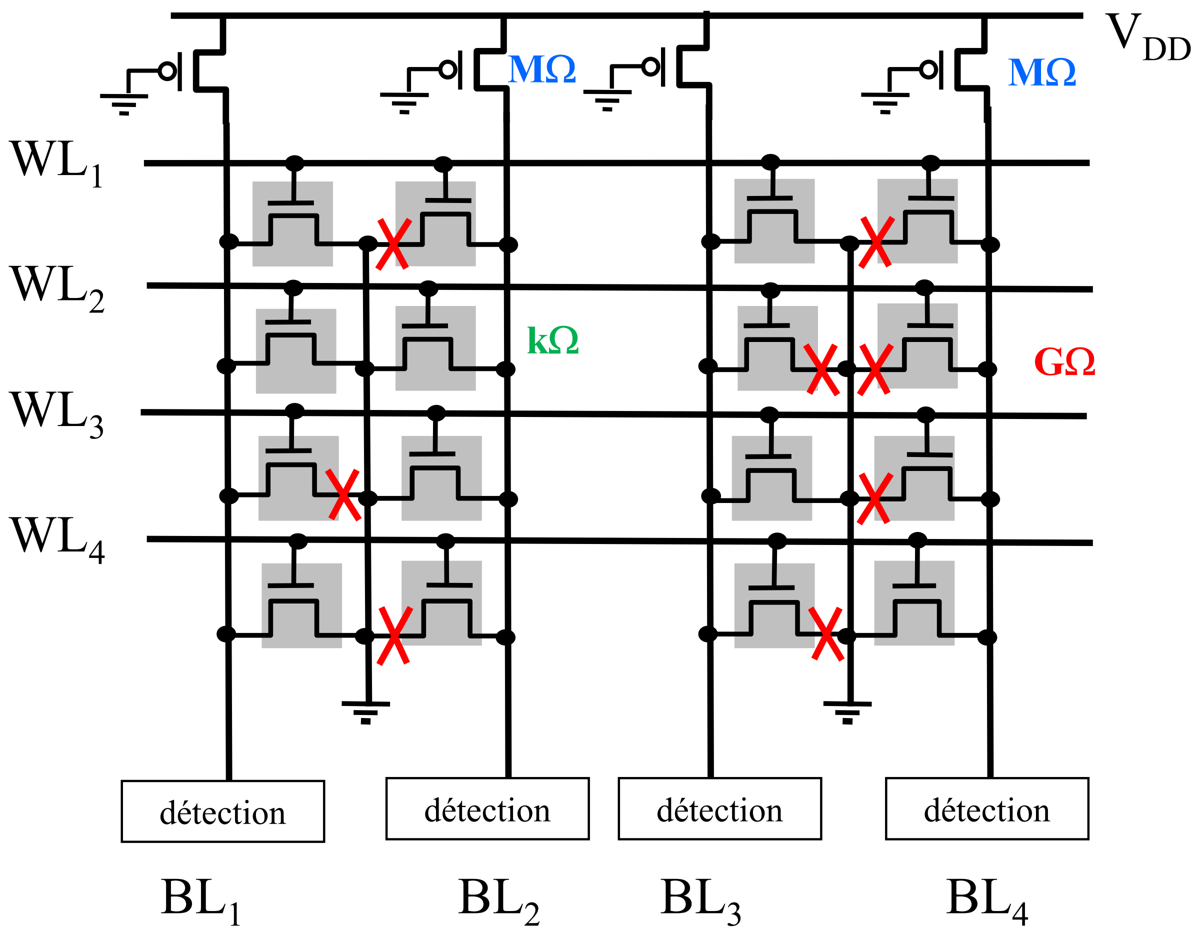


WL 1	WL 2	WL 3	WL 4	BL 1	BL 2	BL 3	BL 4
0				0	1	0	1
	1			0	0	1	1
		0		1	0	0	1
			0	0	1	1	0

Configuration “NOR” (les NMOS sont en parallèle)

Écrite lors du design des masques **un transistor = ”0”** **pas de transistor = “1”**

Mémoires non-volatiles: PROM



Configuration “NOR”

Écrite par post-processing:

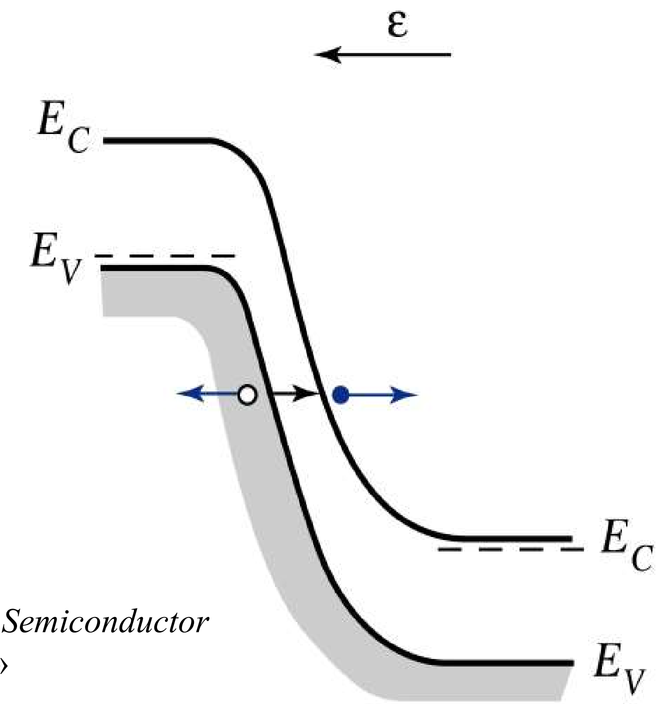
- **Cut laser,**
- **“Fusible”**

un transistor = ”0” **pas de transistor = “1”**

PAB

Floating gate: Résumé: effet tunnel

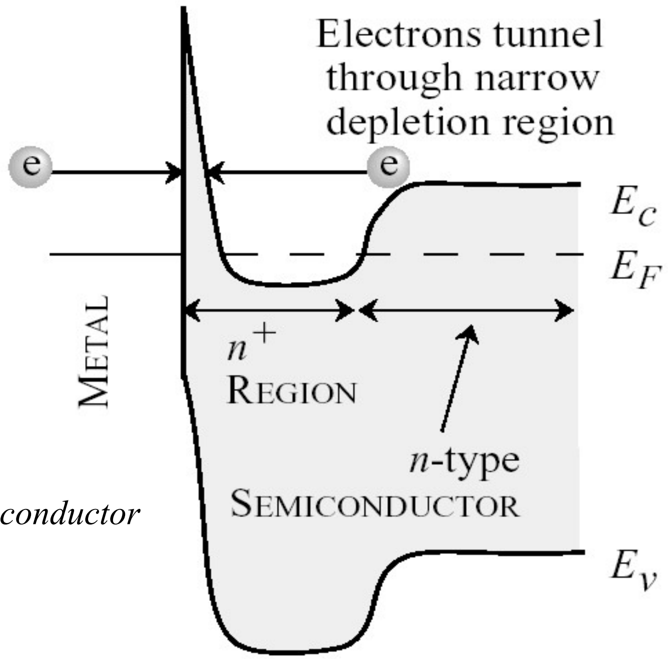
A) Breakdown d'une jonction p/n



S. Sze « *Semiconductor devices* »

$\lambda_e \cong 1\,nm$

B) Contact ohmique

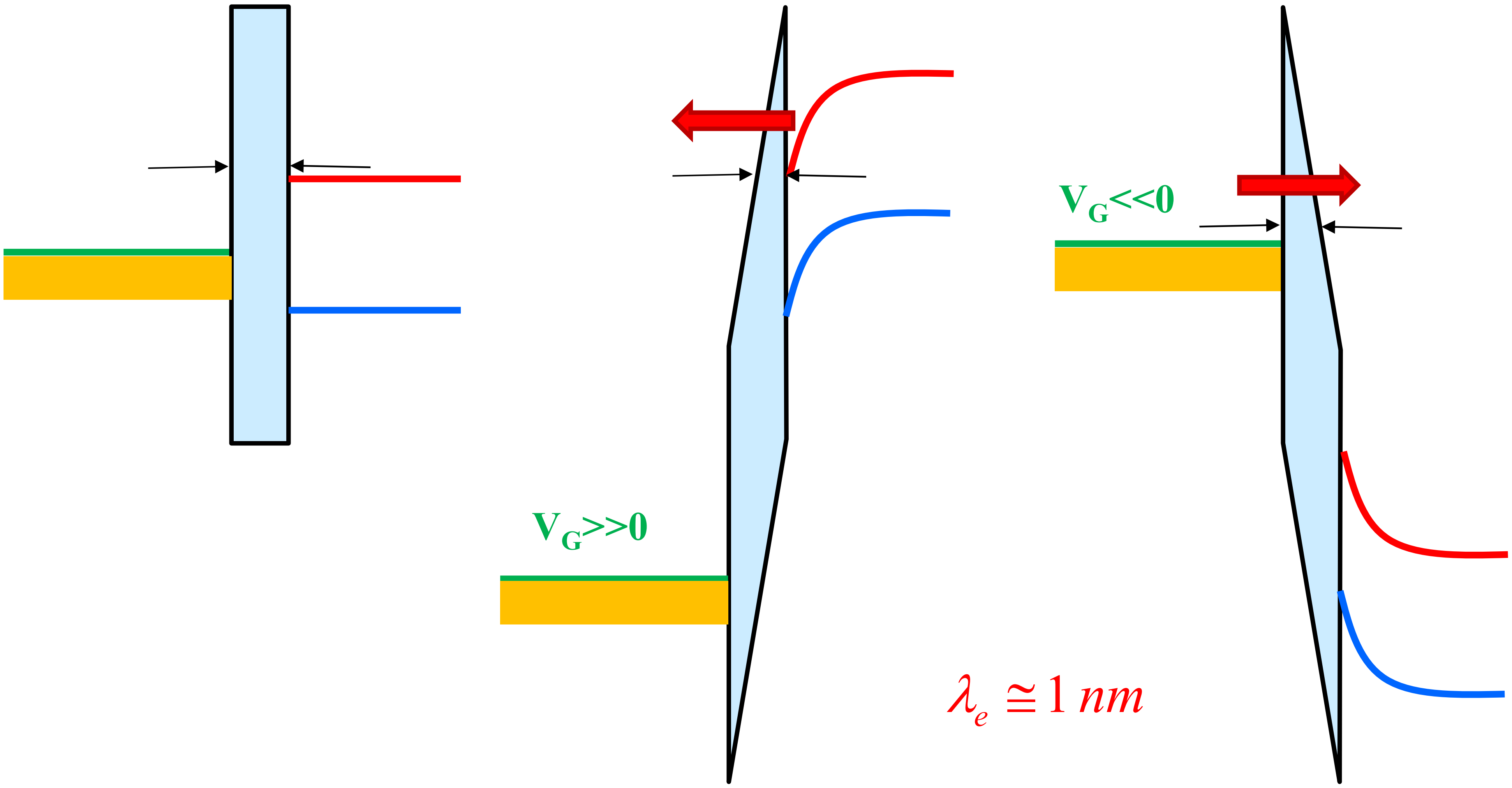


J. Singh « *Semiconductor devices* »

Effet « tunnel »:
L'onde de probabilité pénètre dans la barrière de potentiel par ondes évanescentes.
Si elle est suffisamment mince, l'électron peut traverser.

La jonction métal/semi-conducteur est très étroite.
Les électrons peuvent la traverser sans la voir par effet tunnel.

Effet tunnel sous fort champ électrique: Fowler-Nordheim tunneling



$\lambda_e \cong 1\,nm$

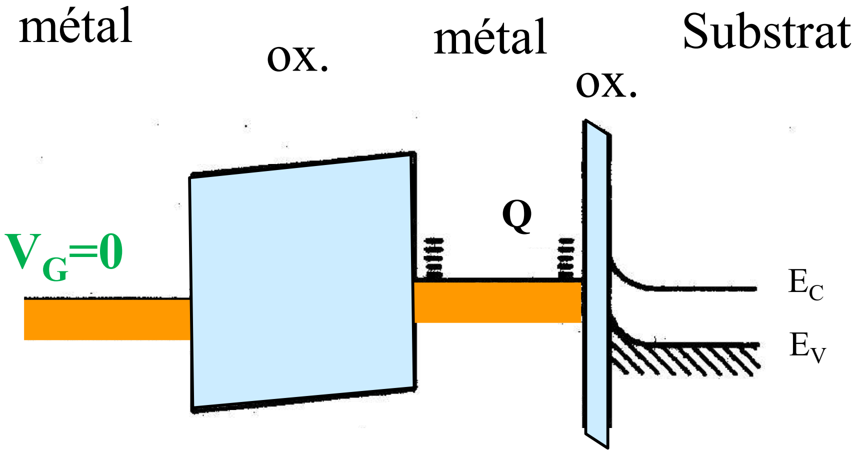
Le champ réduit l'épaisseur de la barrière énergétique

Mémoires non-volatiles: floating gate et effet tunnel

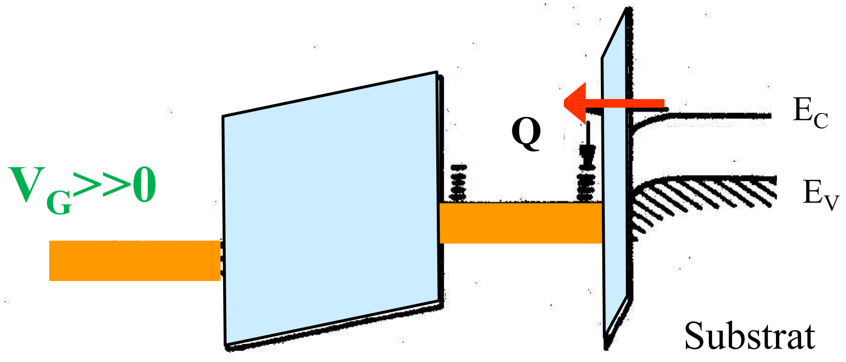
S. Sze « *Physics of semiconductor devices* »

Principe:

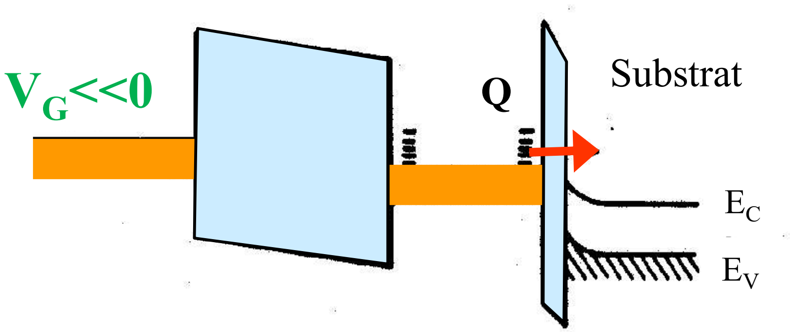
L'effet tunnel dans l'oxyde augmente fortement avec un grand champ électrique.



Conservation des charges: $V_G=0$



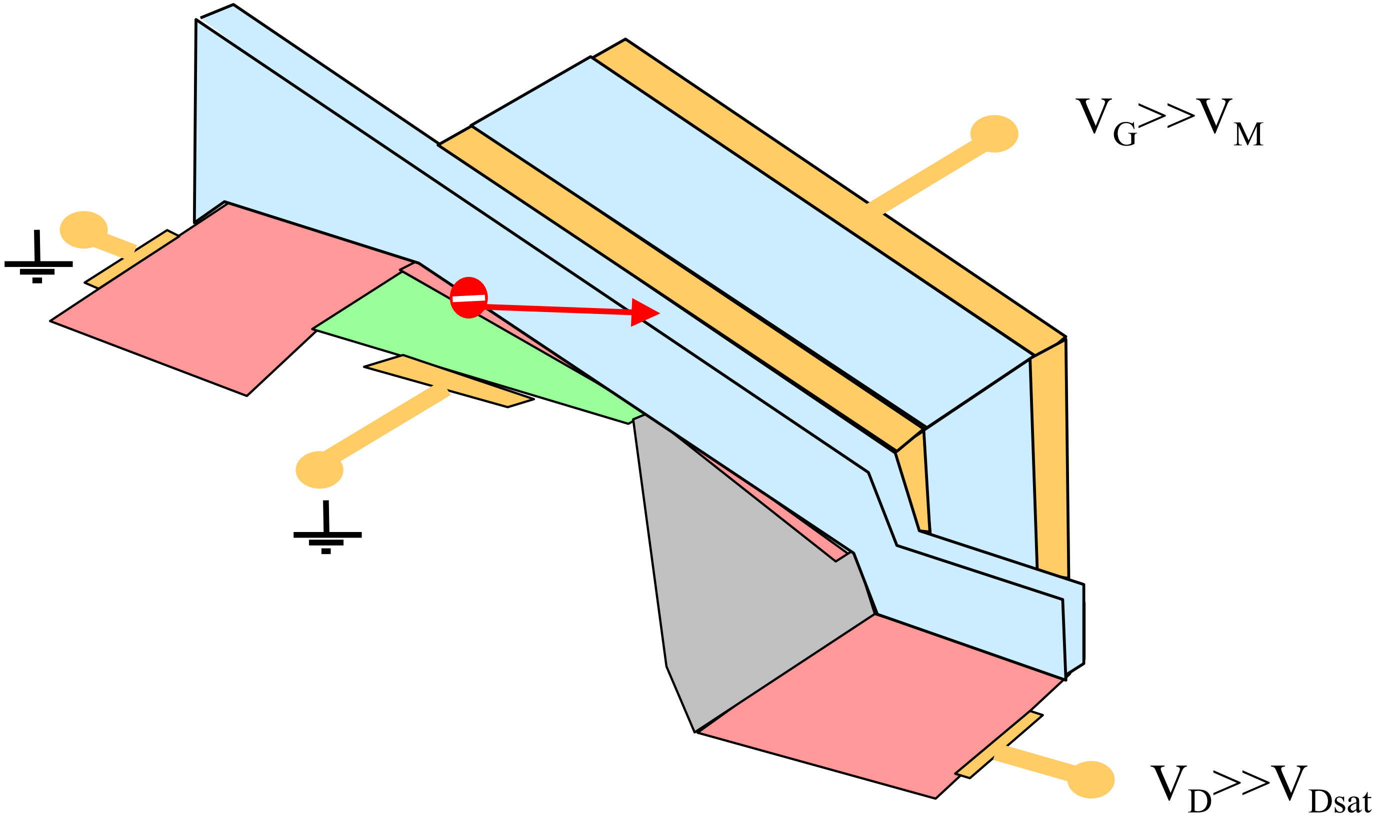
Écriture: $V_G>>0$

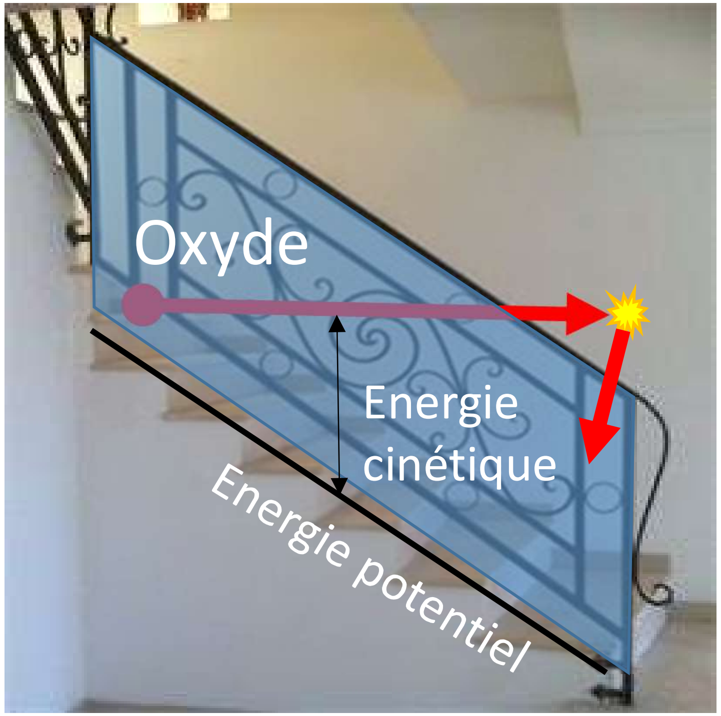


Effacer: $V_G<<0$

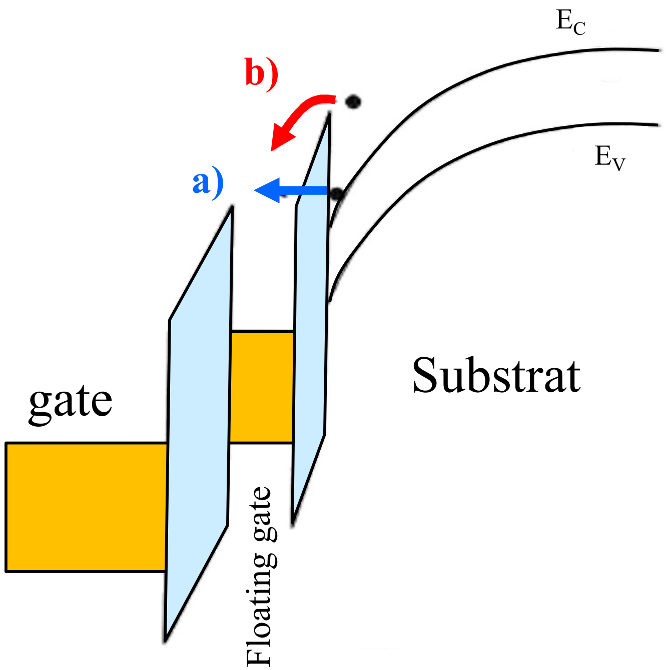
PAB

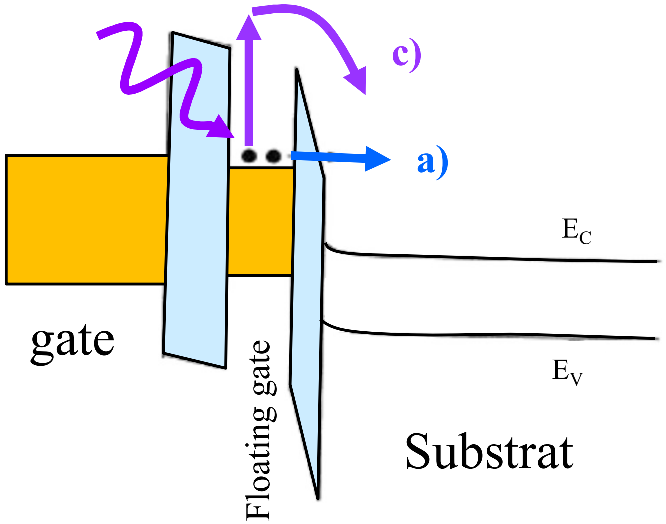
Mémoires non-volatiles: floating gate et «hot electrons»





Floating gate transistor: écrire et effacer



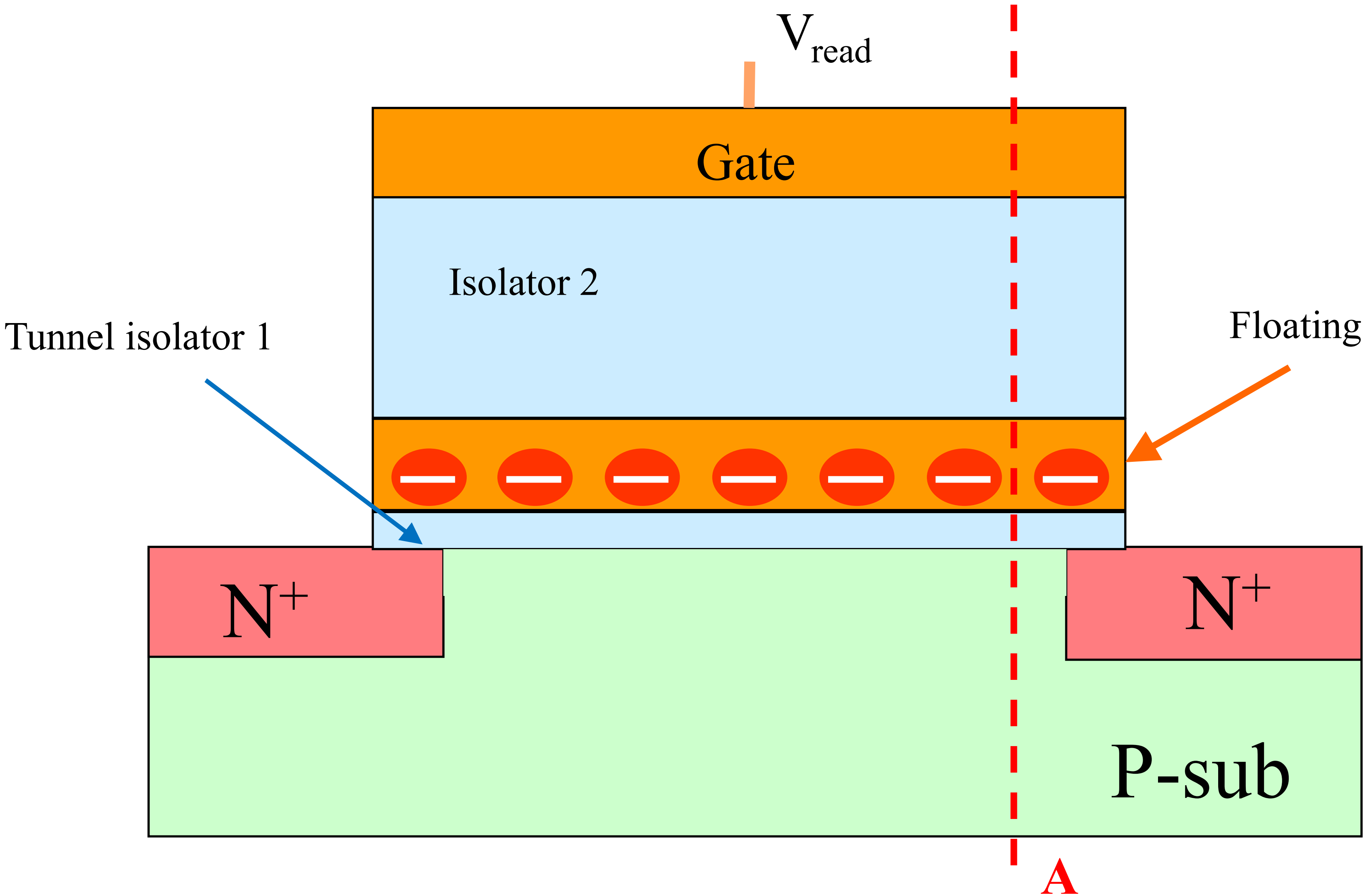


Écrire:
a) Fowler-Nordheim tunneling
b) Hot electrons

Effacer:
a) Fowler-Nordheim tunneling
c) UV illumination

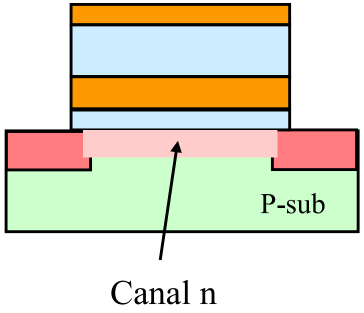
Basé sur S.M. Sze, “Physics of semiconductor devices”, Wiley

Floating gate memories: structure

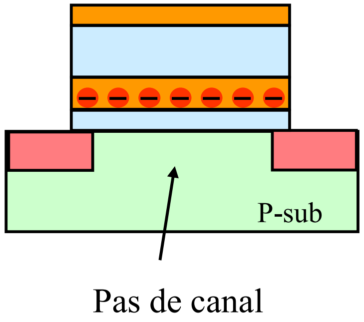


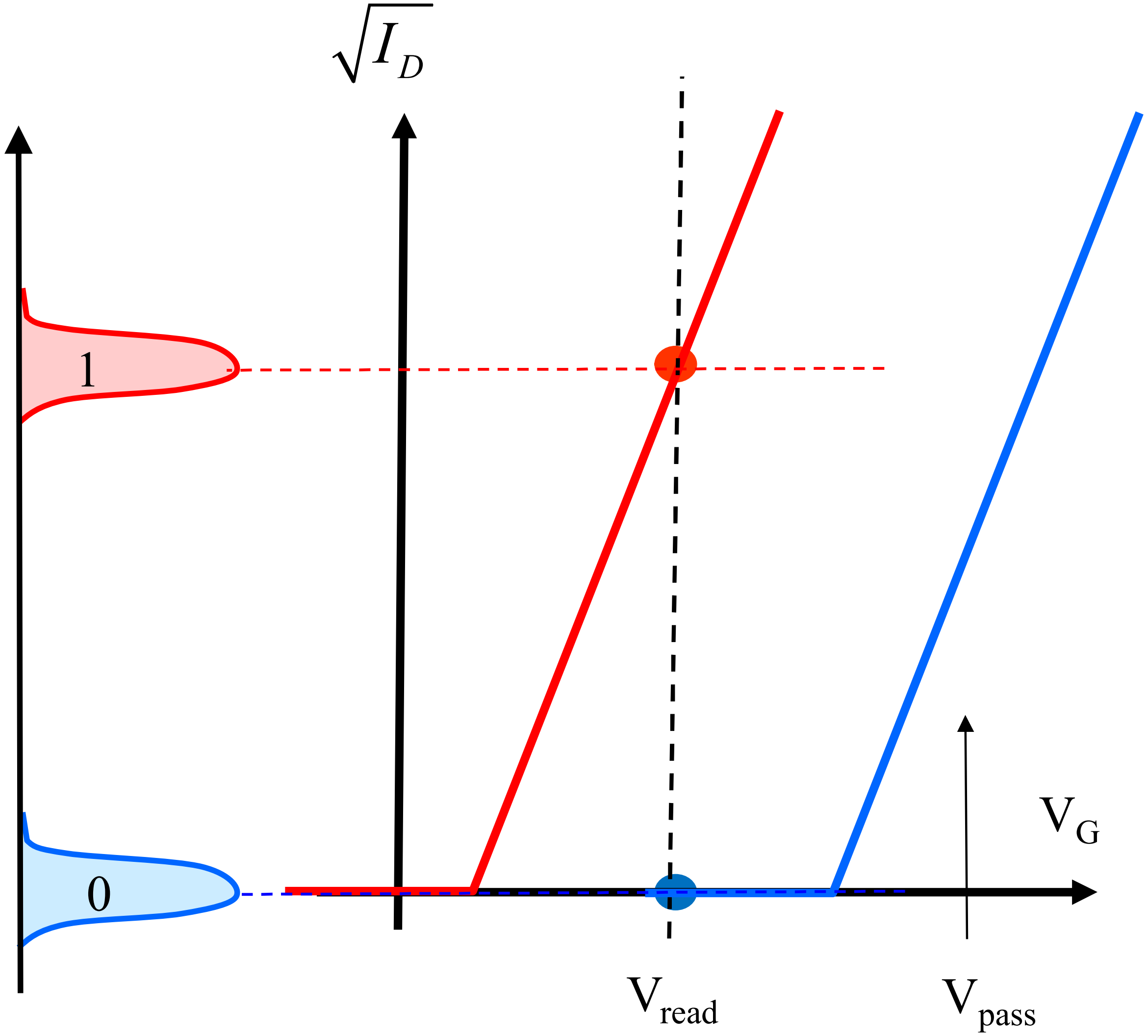
Floating gate memories: (Solid-State Drive SSD) lecture

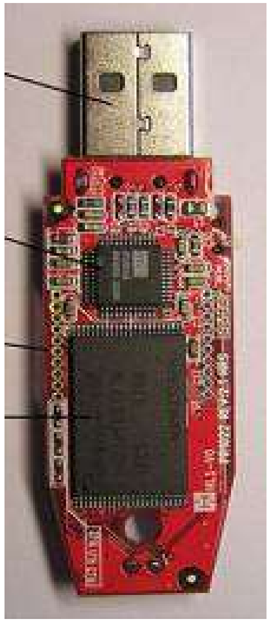
“1” state

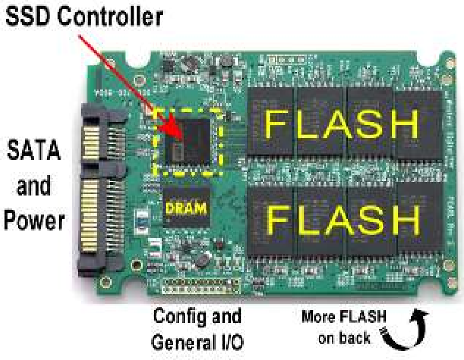


“0” state

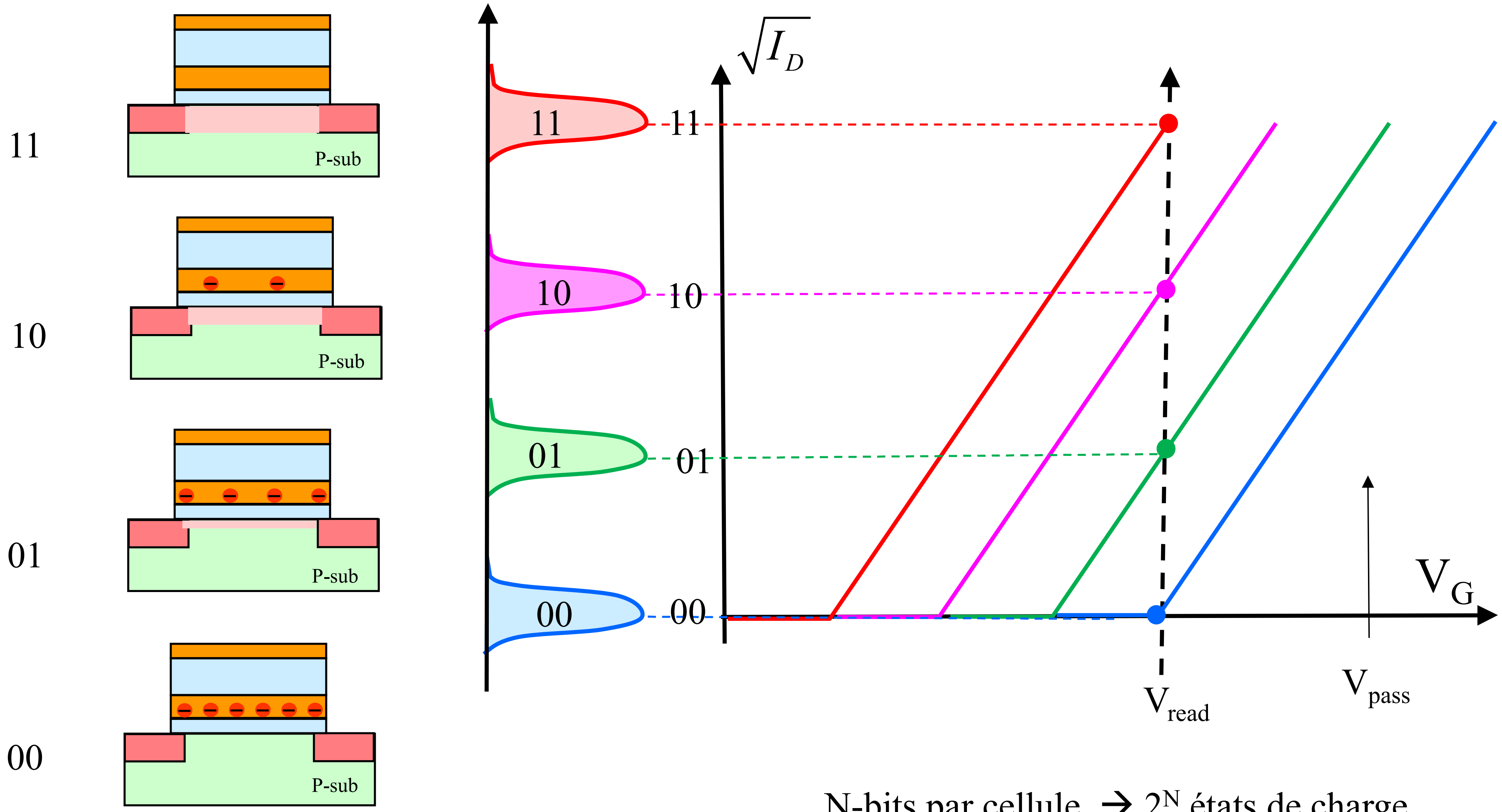








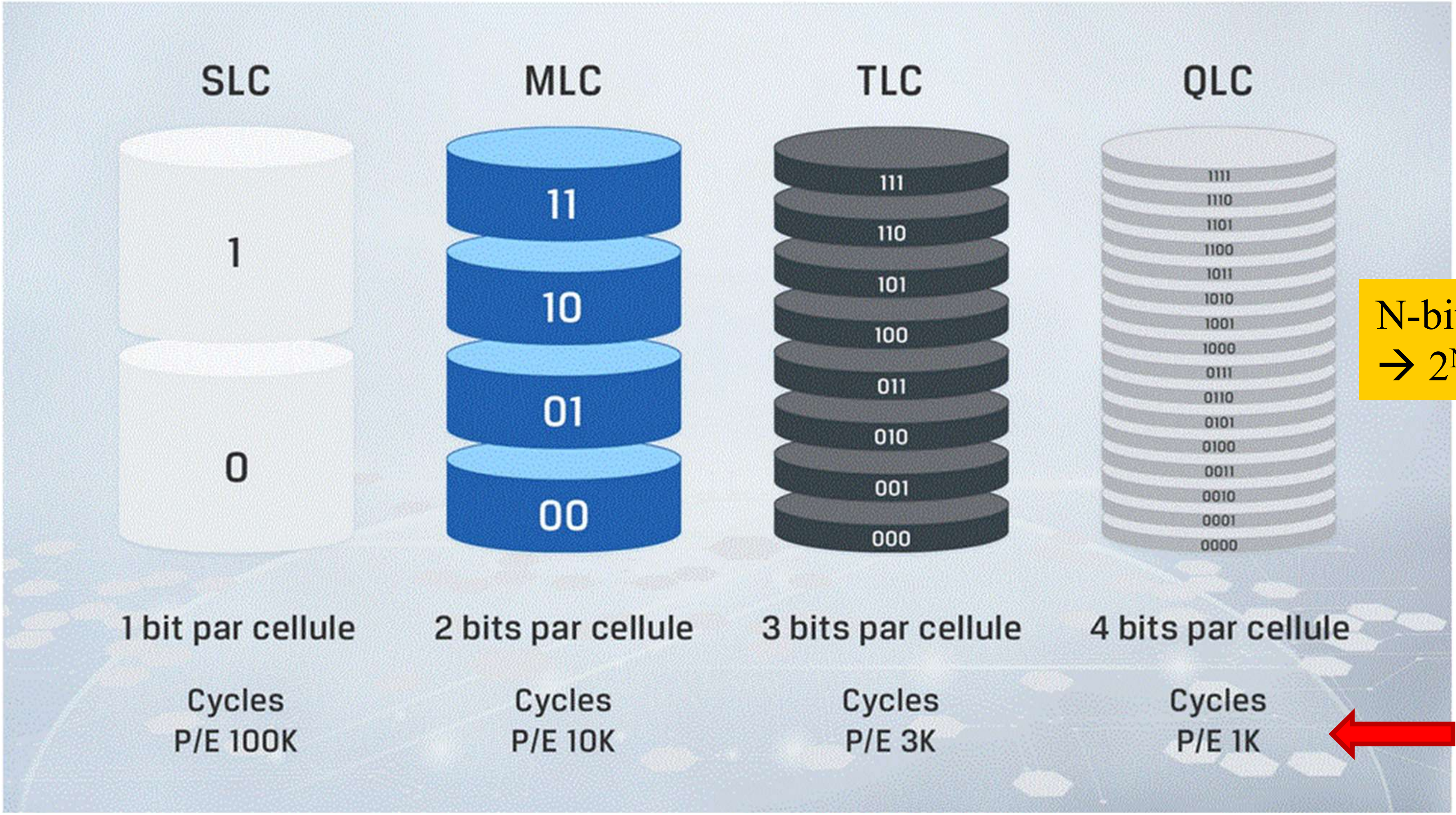
Single-Level Cells (SLC) et Multi-Level Cells (MLC)



N-bits par cellule → 2^N états de charge

Exemples

https://www.kingston.com/fr/blog/pc-performance/difference-between-slc-mlc-tlc-3d-nand



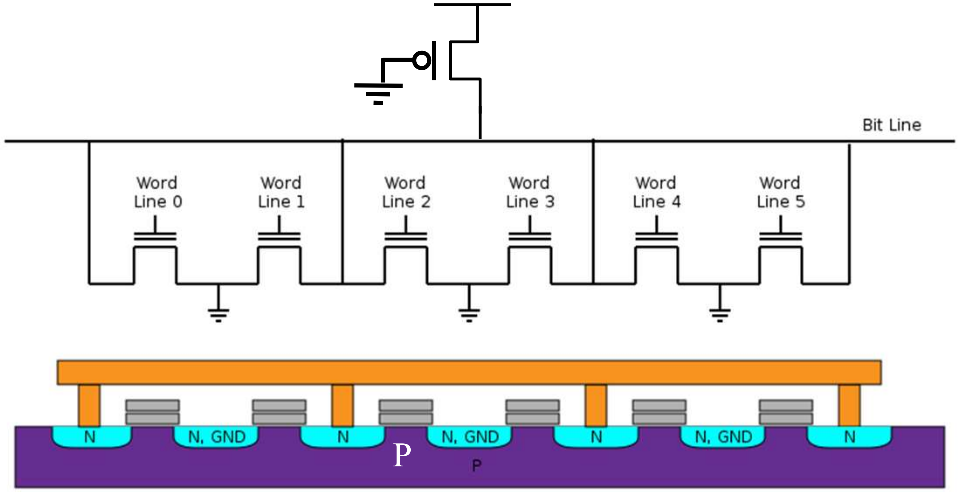
N-bits par cellule
→ 2^N états de charge

P/E = Program/Erease cycle

Schéma des structures NOR et NAND

- Lecture rapide
- Très fiable

→ Remplacement des PROM



By wikipedia user Cyferz, CC BY-SA 3.0, https://commons.wikimedia.org/w/index.php?curid=4571194

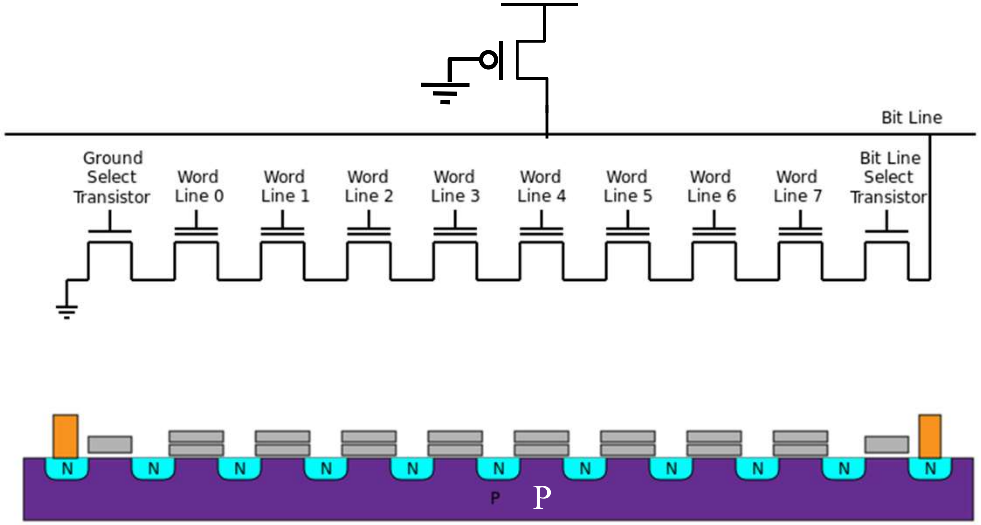
Configuration NOR

NMOS en parallèle

Typique: 2 Gbyte

- Grande densité
- Effacement et écriture rapide

→ SSD
→ Clés USB



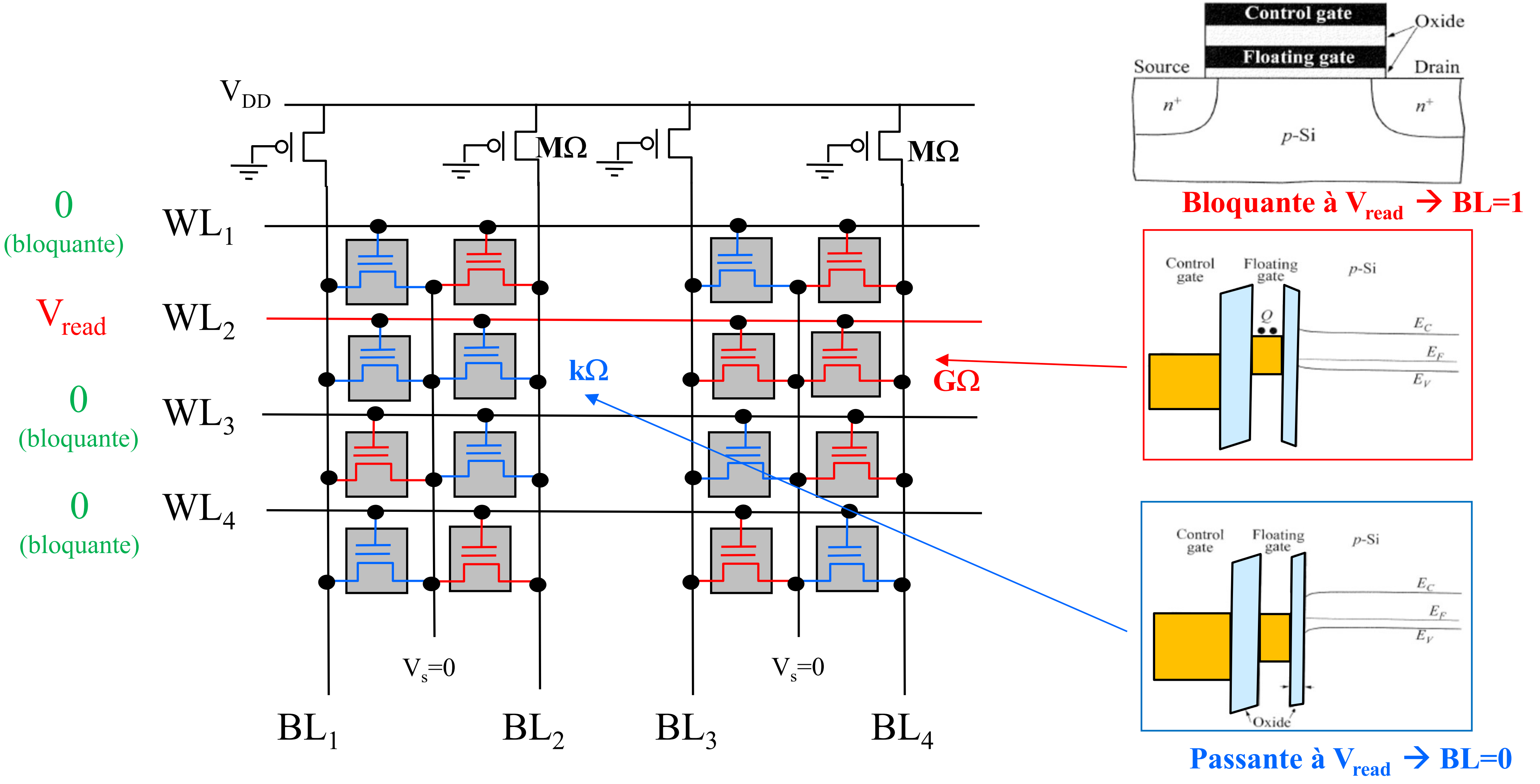
By wikipedia user Cyferz, CC BY-SA 3.0, https://commons.wikimedia.org/w/index.php?curid=4571172

Configuration NAND

NMOS en série

Typique: 2 Tbyte

Mémoires “flash”: Configuration “NOR”

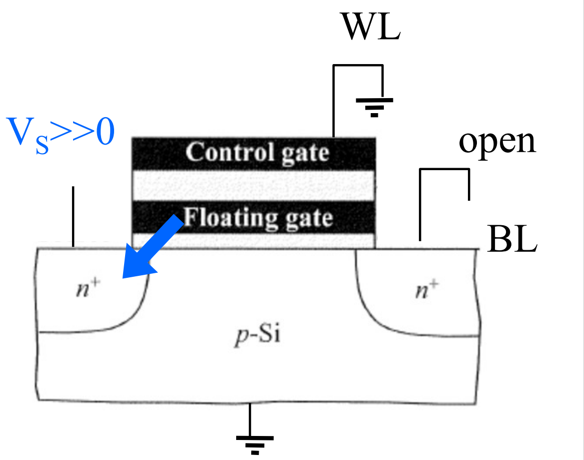


Bloquante à V_{read} → BL=1

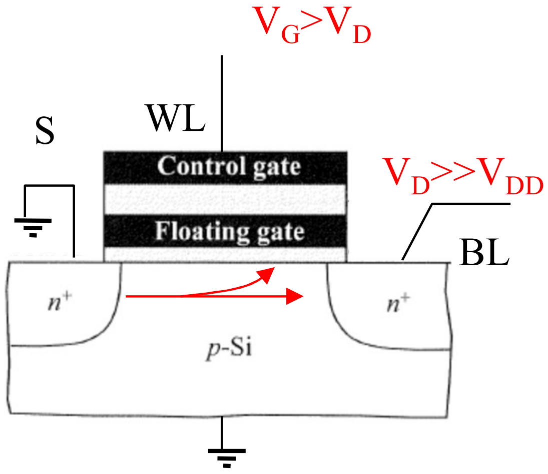
Passante à V_{read} → BL=0

Écrites cellule par cellule, effacées en bloc

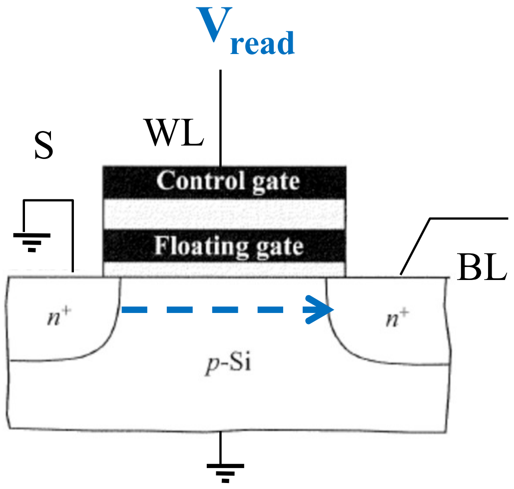
Mémoire “flash” NOR: effacer - écrire - lire



Effacer:
Tunneling



Ecrire:
hot electrons

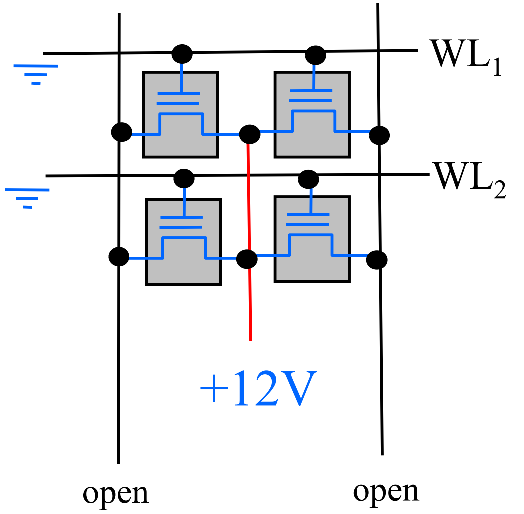


Lire:
MOS ouvert ou fermé

EPROM = «Electrically Programmable ROM»: effacée globalement par UV
EEPROM = “Electrically Erasable PROM” effacée cellule par cellule, mais 2T par cellule
Flash = EPROM effaçable électriquement par region

Mémoires “flash” NOR: effacer - écrire - lire

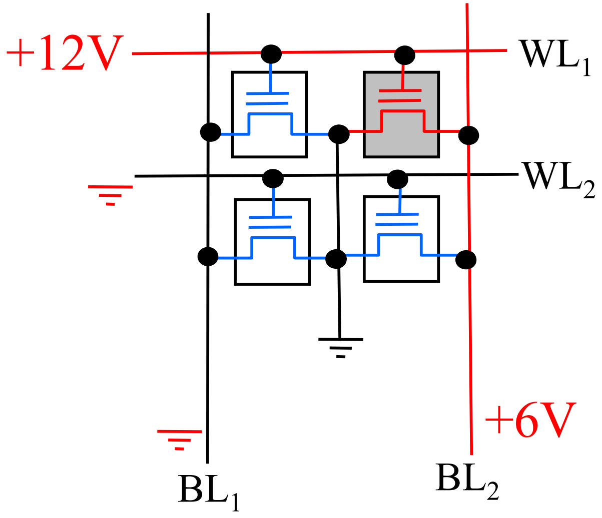
Tunneling du floating gate vers la source



Effacer

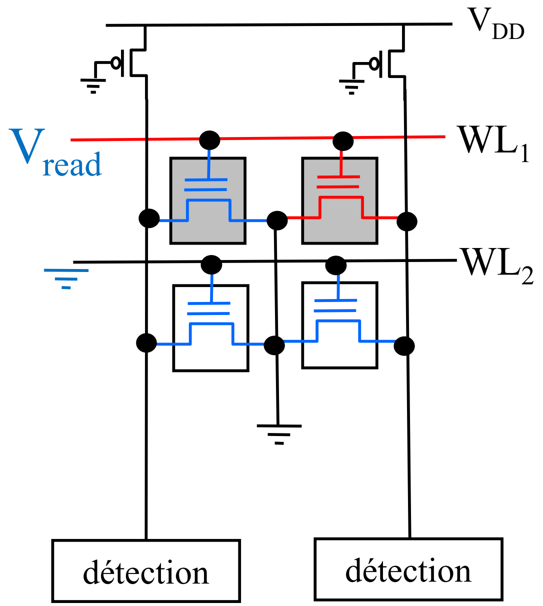
Décharger toutes les cellules

Hot electrons



Ecrire

Mettre une charge sur la cellule

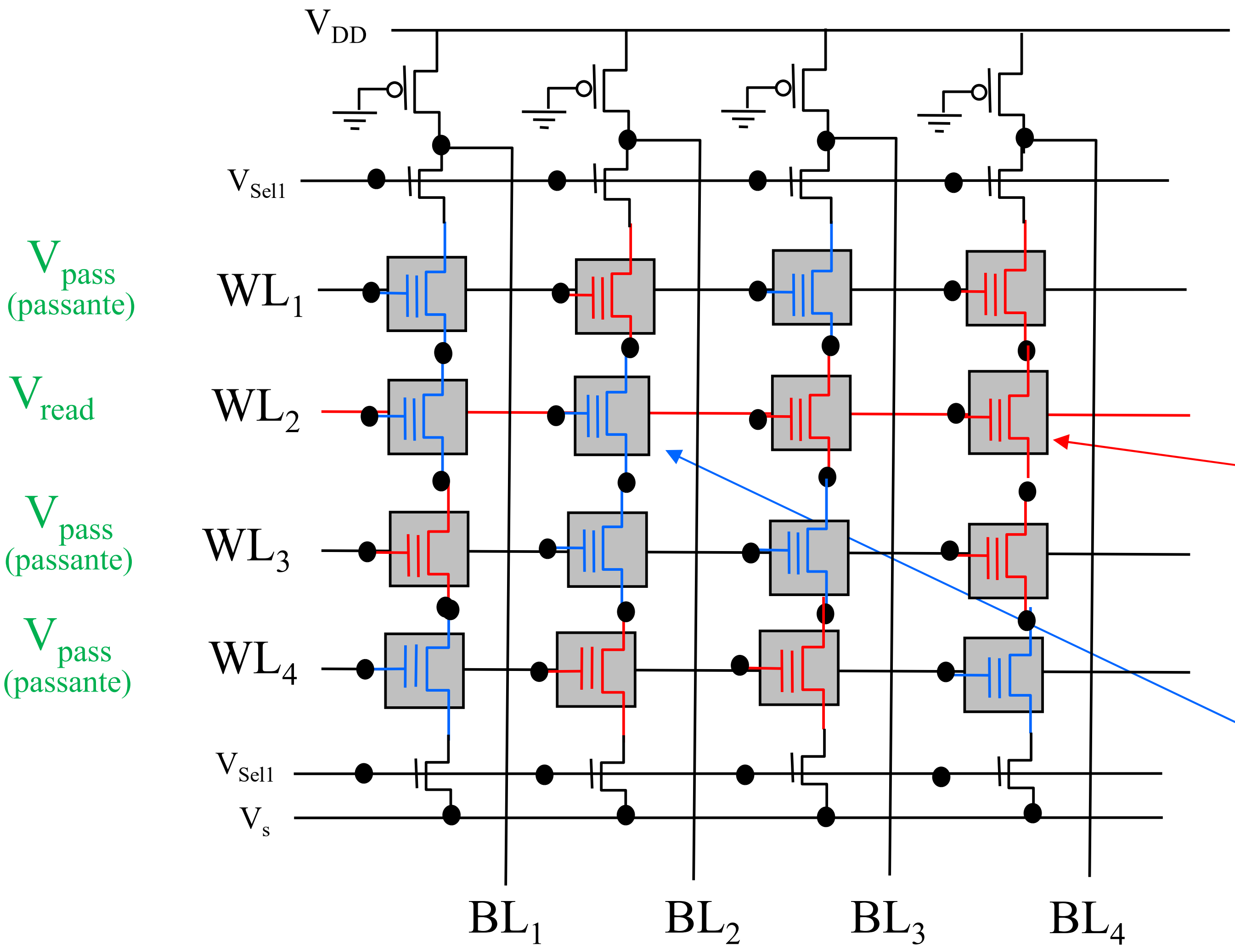


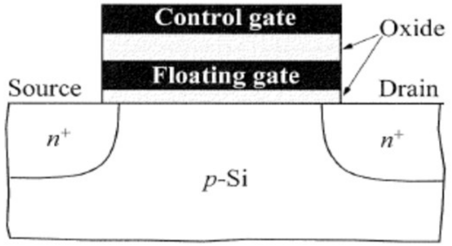
Lire

Toutes les cellules en même temps

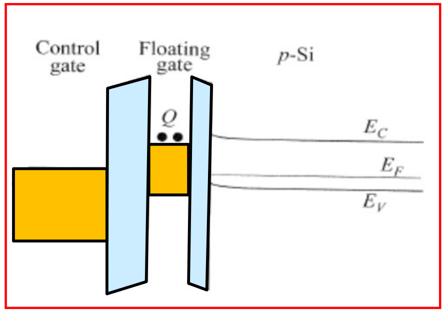
Accès à chaque cellule séparément

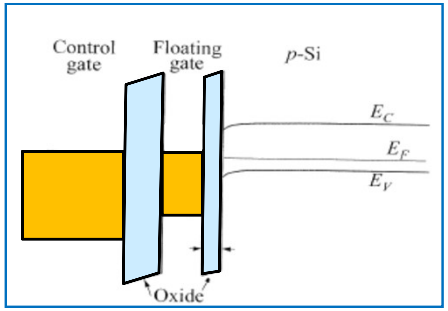
Mémoires “flash”:
Configuration “NAND”: Typique: 32 WL et 2^{16} BL par bloc





Bloquante à V_{read} → BL=1





Passante à V_{read} → BL=0

Écrites cellule par cellule, effacées en bloc

PAB

Exercice E11.1: Contrôle de la tension de threshold V_{M0}

a) Dessinez le schéma de bande d’une jonction MOS sur substrat p le long d’une droite verticale au milieu du gate à la tension $V_G=V_{M0}$.

b) Considérons une augmentation de l’épaisseur de l’oxyde, tout en maintenant la structure au threshold:

- Comment varient le potentiel de surface, les charges d’espace dans la zone de déplétion, ainsi que le champ électrique dans l’oxyde.
- Comment varie la tension de threshold appliquée sur le gate ?

c) Repartons de la situation a) et considérons maintenant une augmentation du dopage p du substrat, tout en maintenant la structure au threshold. Négligez la variation de ψ_B.

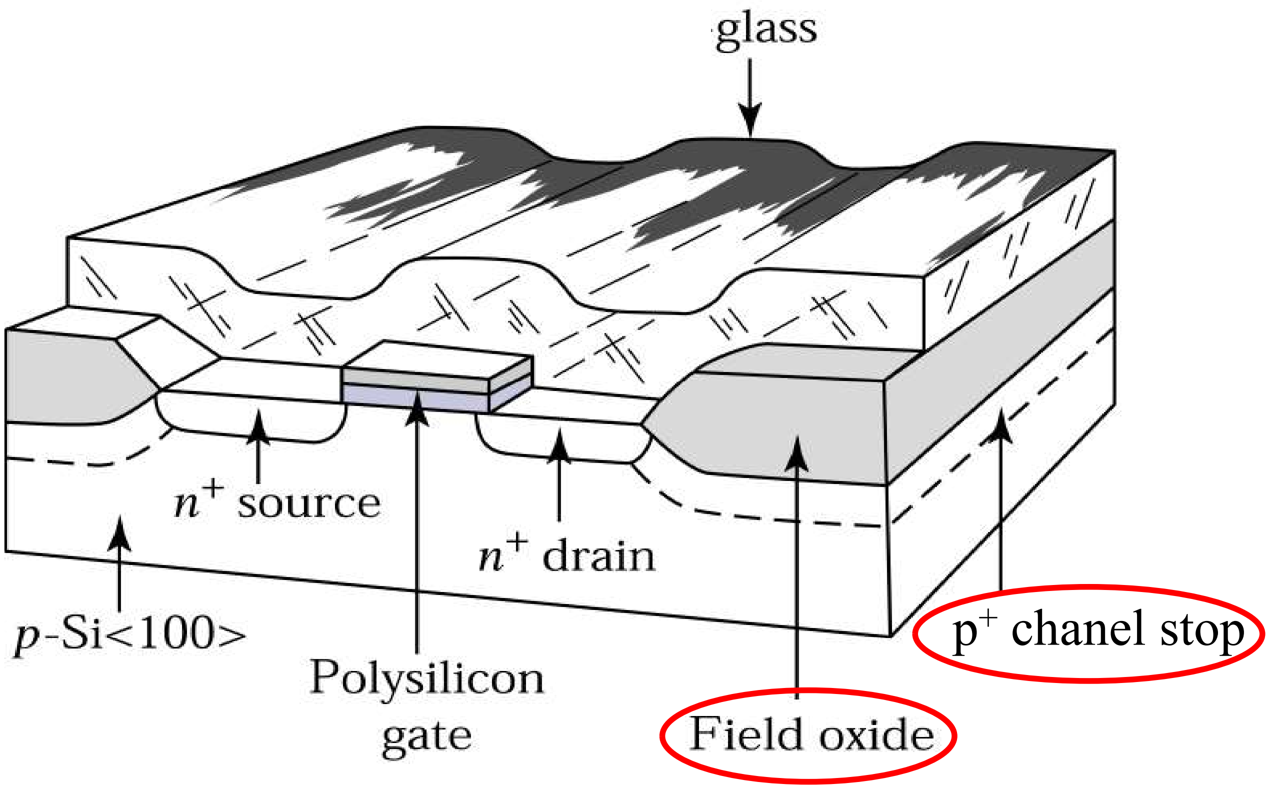
- Comment varient le potentiel de surface, les charges d’espace dans la zone de déplétion, le champ à l’interface semi-conducteur/oxyde ainsi que le champ électrique dans l’oxyde.
- Comment varie la tension de threshold appliquée sur le gate ?

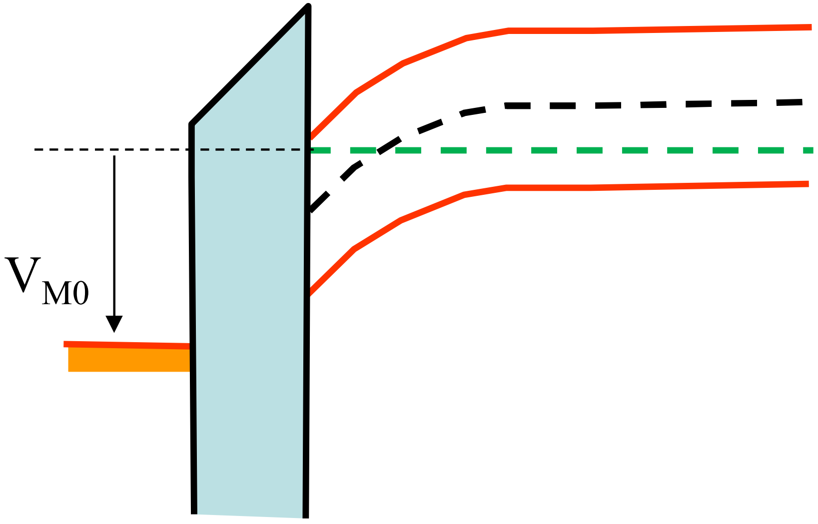
Idée: Commencez votre analyse pour b) et c) à partir de la profondeur du substrat.

d) Comparez vos résultats avec le cours chapitre 11!

Exercice E11.1:
Contrôle de la tension de threshold V_{M0}

Semiconductor Devices, 2/E by S. M. Sze





$$V_{M0} = V_{fb} + 2\psi_B \left(1 + 2\frac{C_{B,th}}{C_{ox}}\right)$$

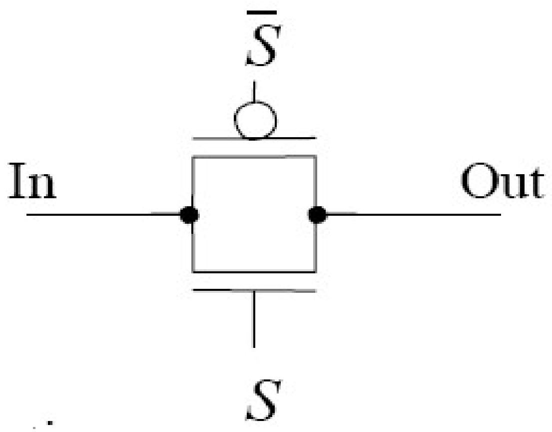
d_{ox} ↗

N_A ↗

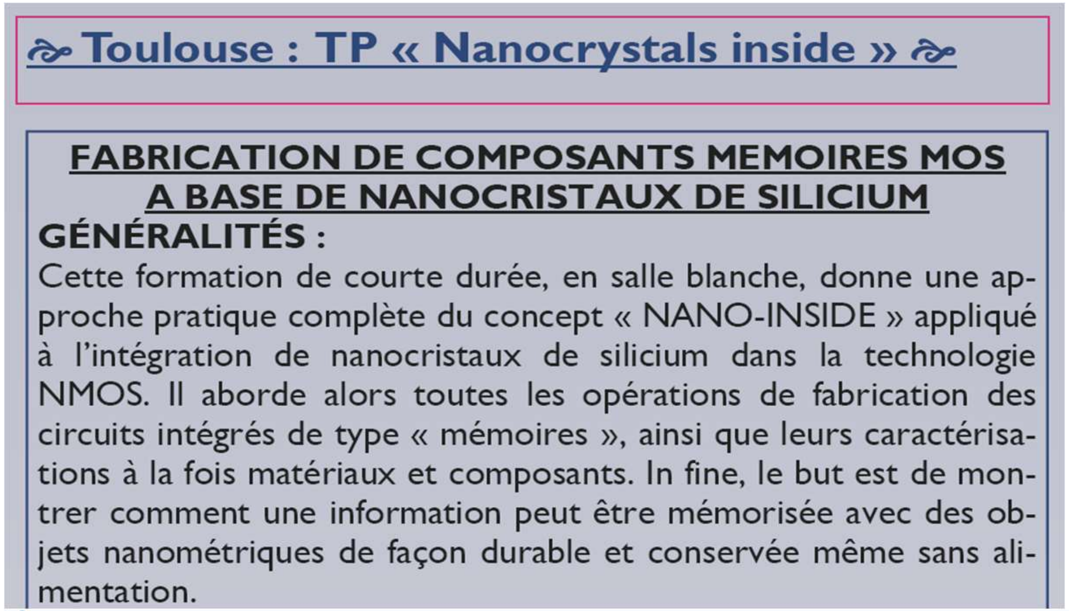
Exercices E11.2

E11.2: Transmission gate

- Considérez le circuit ci-contre. Les signaux sont digitaux. Trouvez la table de vérité donnant la sortie « out » en fonction de l'entrée « in » et du signal de contrôle « S ».
  « $\overline{S}$ » est l'inverse binaire de « S ».
- Pourquoi le PMOS est-il nécessaire ?



Exercice 11.4:
“Nanocrystals inside”

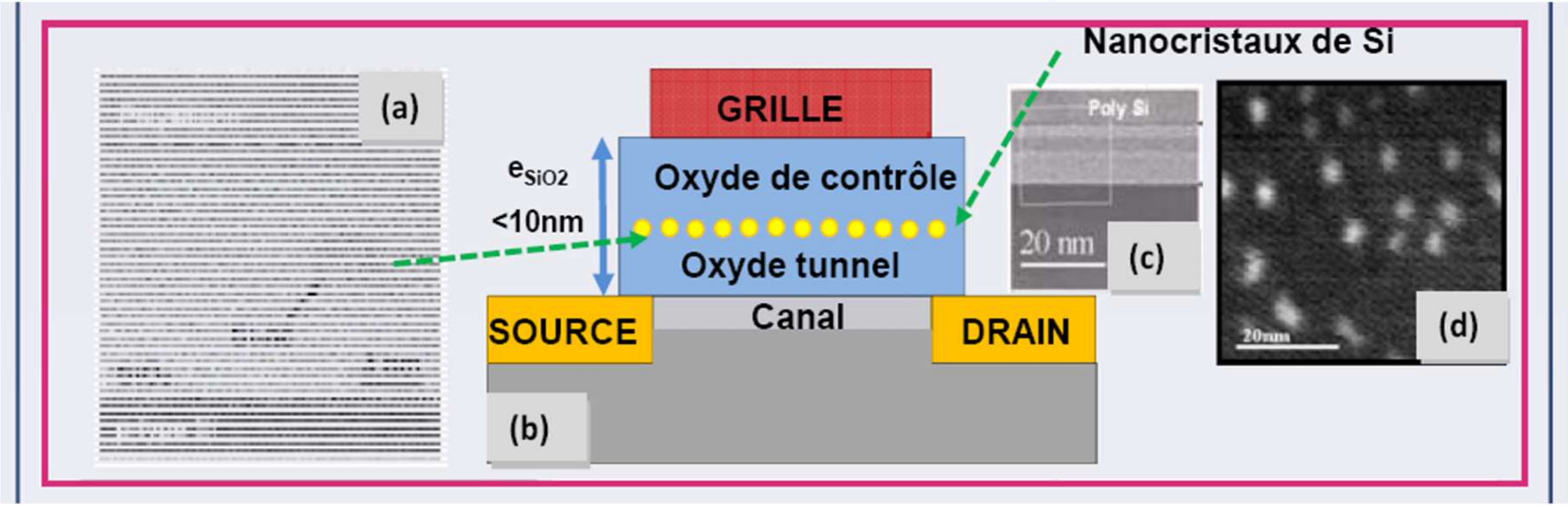


Toulouse : TP « Nanocrystals inside »

FABRICATION DE COMPOSANTS MEMOIRES MOS A BASE DE NANOCRISTAUX DE SILICIUM

GÉNÉRALITÉS :

Cette formation de courte durée, en salle blanche, donne une approche pratique complète du concept « NANO-INSIDE » appliqué à l’intégration de nanocristaux de silicium dans la technologie NMOS. Il aborde alors toutes les opérations de fabrication des circuits intégrés de type « mémoires », ainsi que leurs caractérisations à la fois matériaux et composants. In fine, le but est de montrer comment une information peut être mémorisée avec des objets nanométriques de façon durable et conservée même sans alimentation.



Lisez et interprétez ce texte

La puce à l’oreille
No. 31,
p. 4, nov. 2009.

Exercice 11.5 ISFET

Comment varie la tension de threshold si:

A) la soupe contient des ions positifs (pH<7)
B) la soupe contient des ions négatifs (pH>7)